

Compal confidential

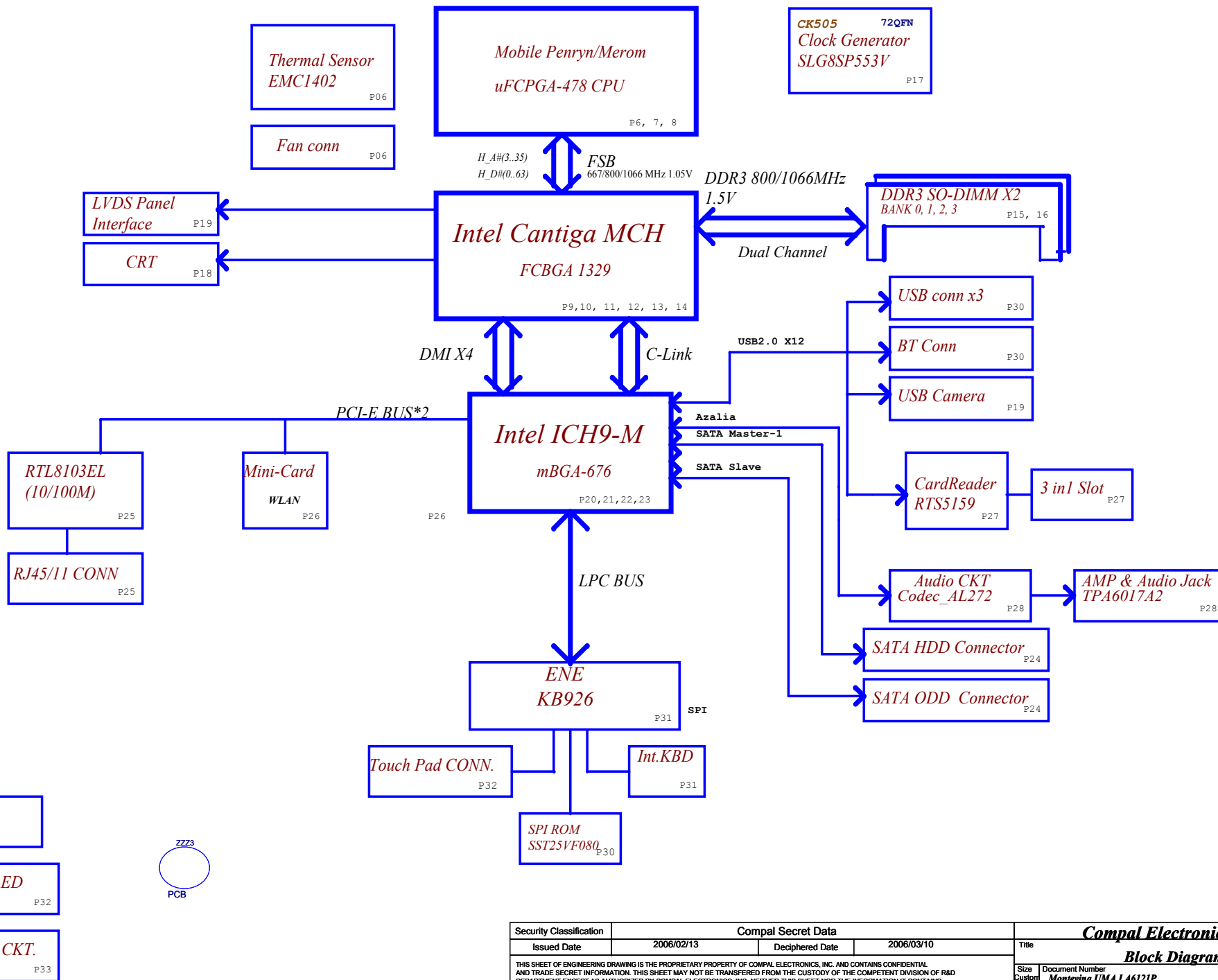
Schematics Document

Mobile Penryn uFCPGA with Intel
Cantiga_GM+ICH9-M core logic

2010-04-08

NCL50 REV:1.0

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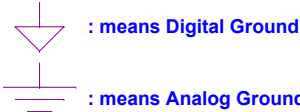
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Voltage Rails

O MEANS ON X MEANS OFF

power plane	State				
		+B	+5VALW +3VALW	+1.8V +1.5V	+5VS +3VS +1.5VS +VCCP +CPU_CORE +0.75VS
S0		O	O	O	O
S1		O	O	O	O
S3		O	O	O	X
S5 S4/AC		O	O	X	X
S5 S4/ Battery only		O	X	X	X
S5 S4/AC & Battery don't exist		X	X	X	X

Symbol Note :



@ :	means just reserve , no build
45@ :	means need be mounted when 45 level assy or rework stage.
DEBUG@ :	means just reserve for debug.
BATT @ :	means need be mounted when 45 level assy or rework stage.
CONN@ :	means ME part

USB assignment:

USB-0	Right side daughter board
USB-0	Right side daughter board
USB-2	Left side
USB-3	X
USB-4	Camera
USB-5	WLAN
USB-6	Bluetooth
USB-7	Cardreader
USB-8	X
USB-9	X
USB-10	X
USB-11	X

PCIe assignment:

PCIe-1	X
PCIe-2	X
PCIe-3	WLAN
PCIe-4	GLAN (Realtek)
PCIe-5	X
PCIe-6	X

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

SMBUS Control Table

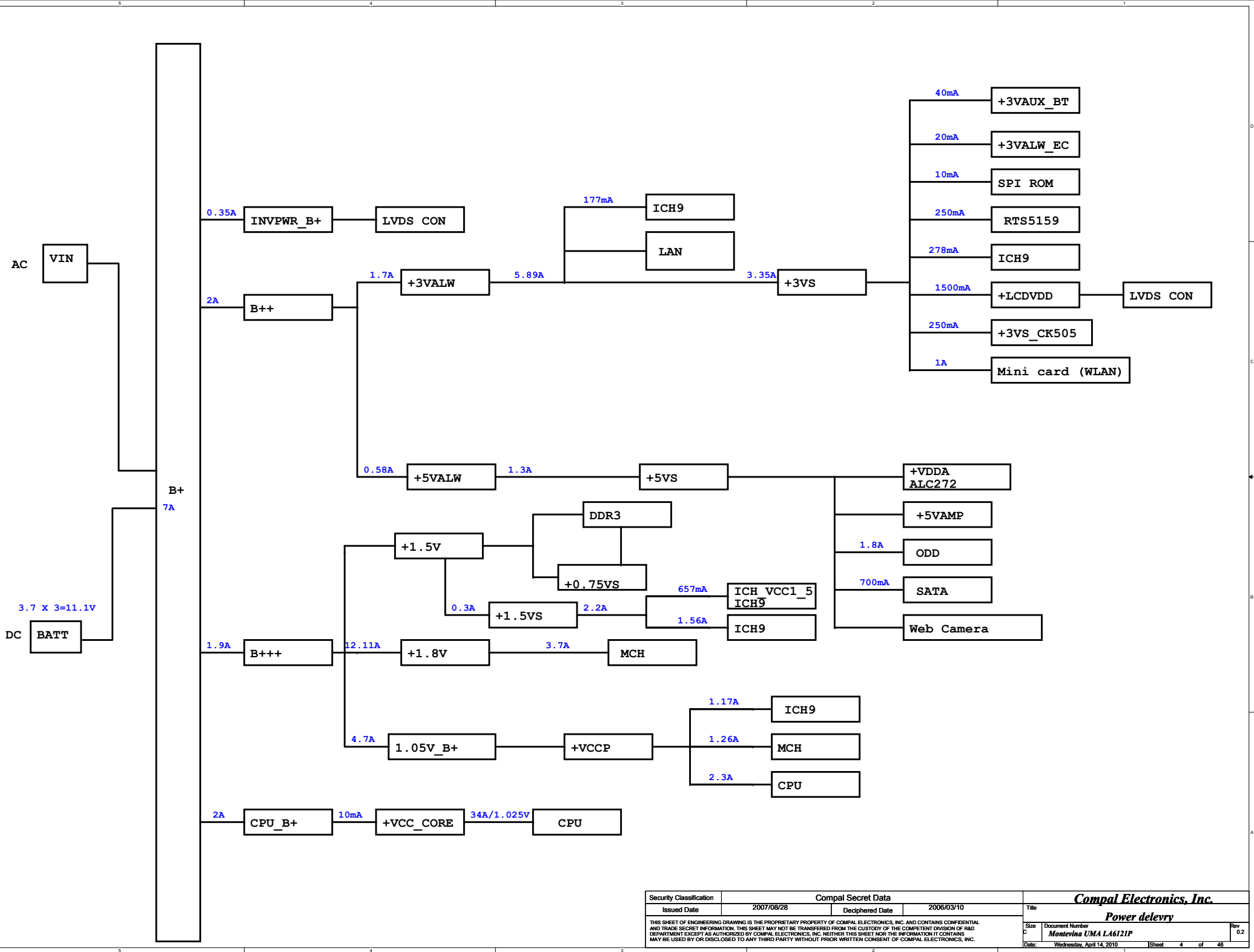
	SOURCE	INVERTER	BATT	SERIAL EEPROM	Thermal Sensor	SODIMM	CLK CHIP	MINI CARD	LCD			
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	X	X	X	X	X	X			
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X			
ICH_SMBCLK ICH_SMBDATA	ICH9	X	X	X	X	V	V	V	X			
DDC2_CLK DDC2_DATA	Cantiga	X	X	X	X	X	X	X	V			

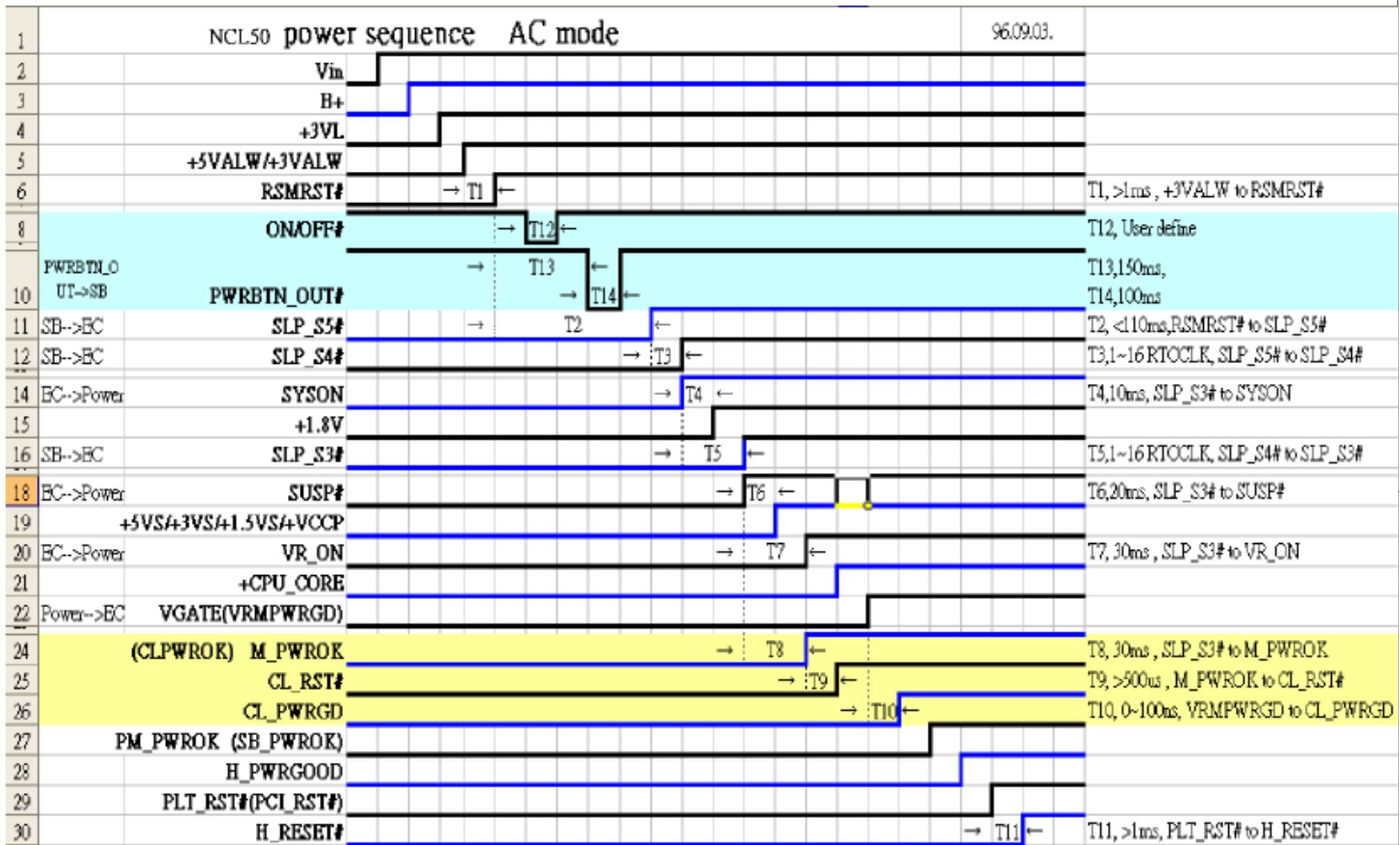
43184330L01 : UMA GL PR FF-

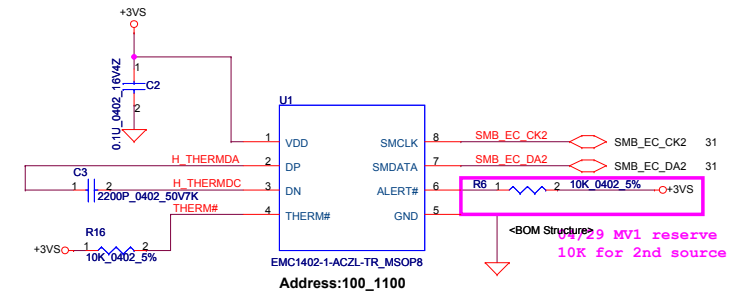
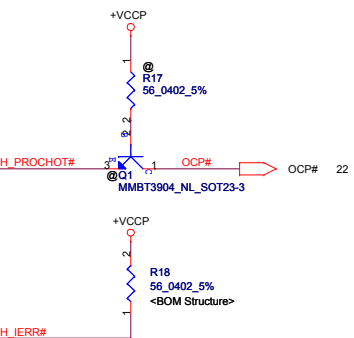
43184330L01 : Main@/DEBUG@/NewC@

PCB : DA60000GI00 --->M/B

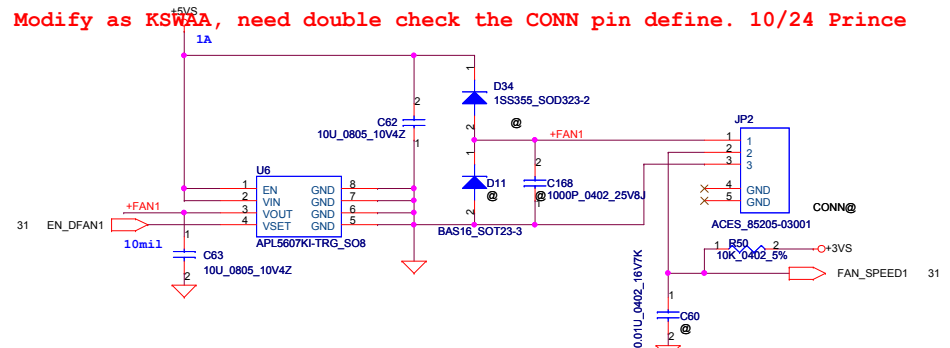
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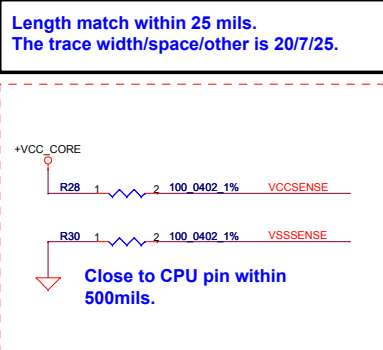
Modify as KSWAA^{+5VS}, need double check the CONN pin define. 10/24 Prince

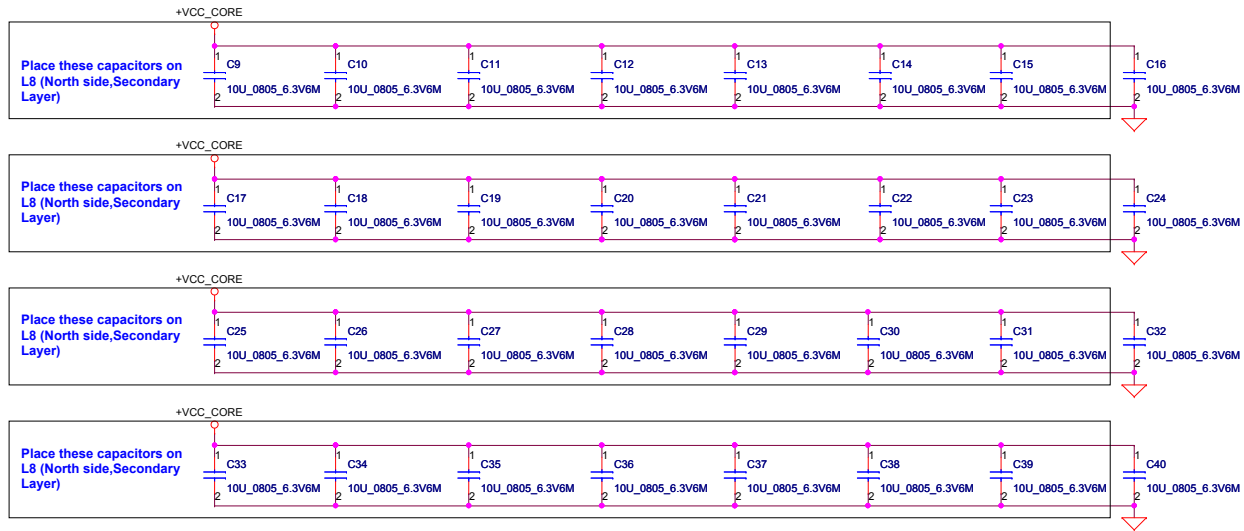
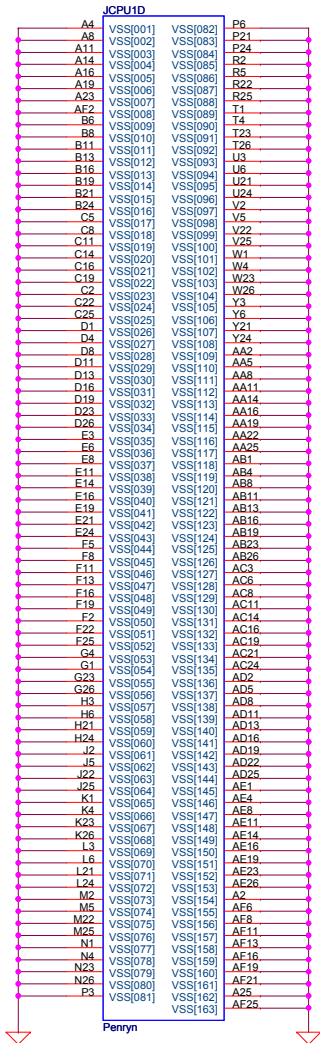




Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.

Close to CPU pin AD26 within 500mils.

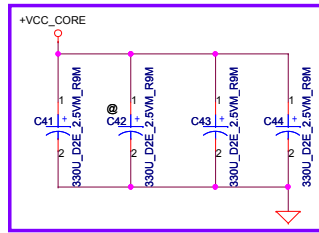




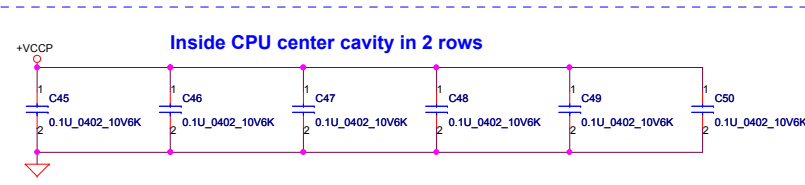
Mid Frequency Decoupling

Near CPU CORE regulator

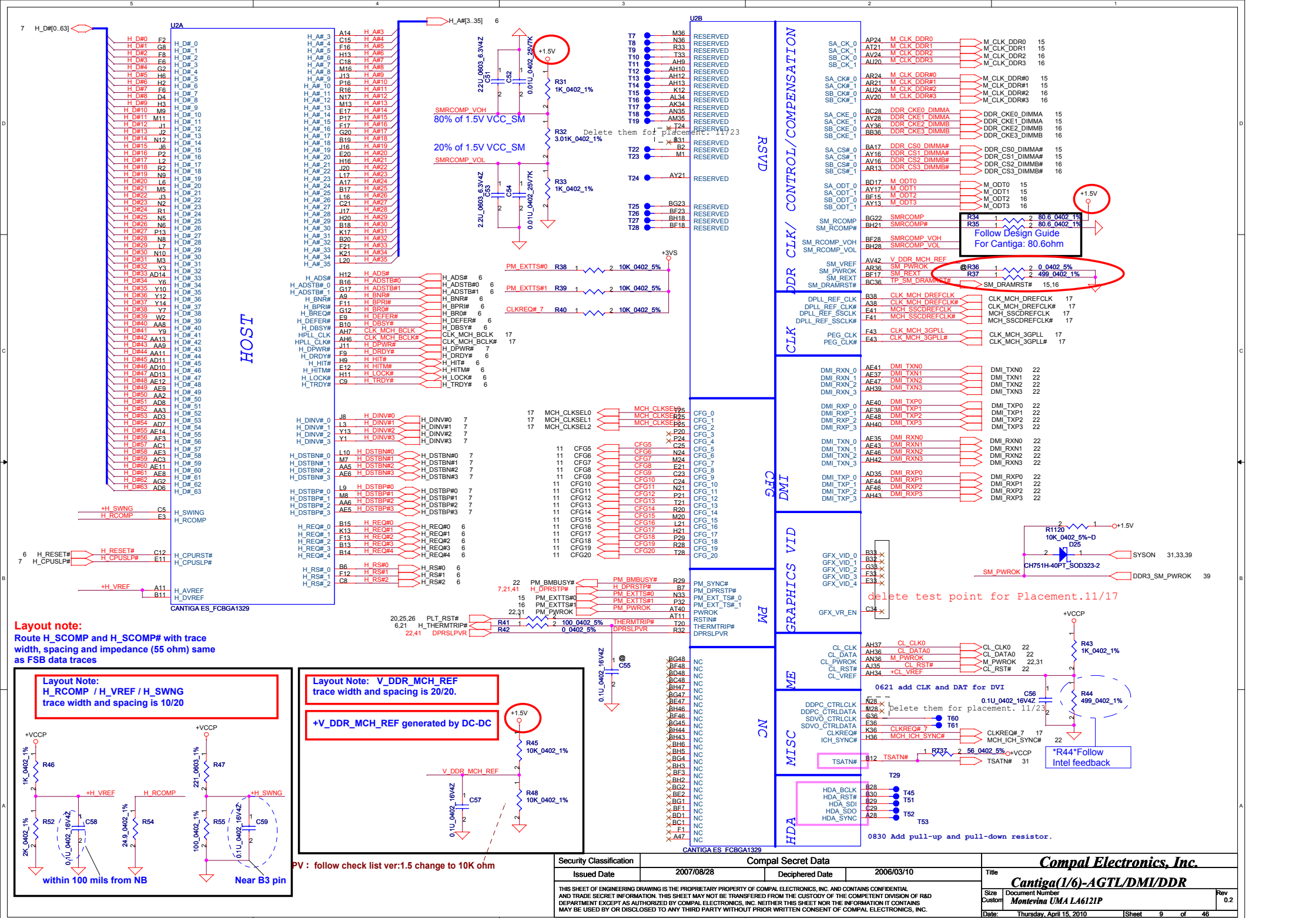
ESR <= 1.5m ohm
Capacitor > 1980uF

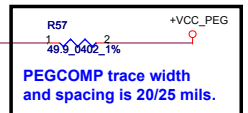
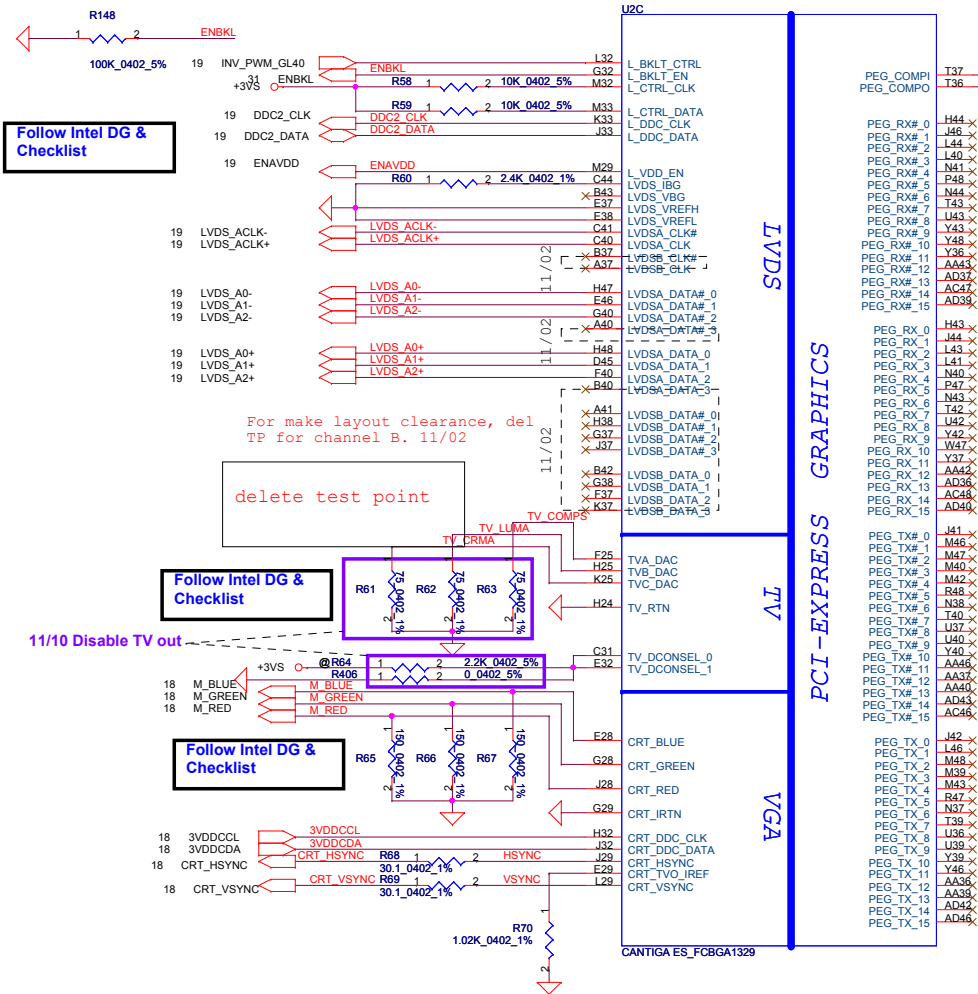


11/21 Change ESR=7m ohm



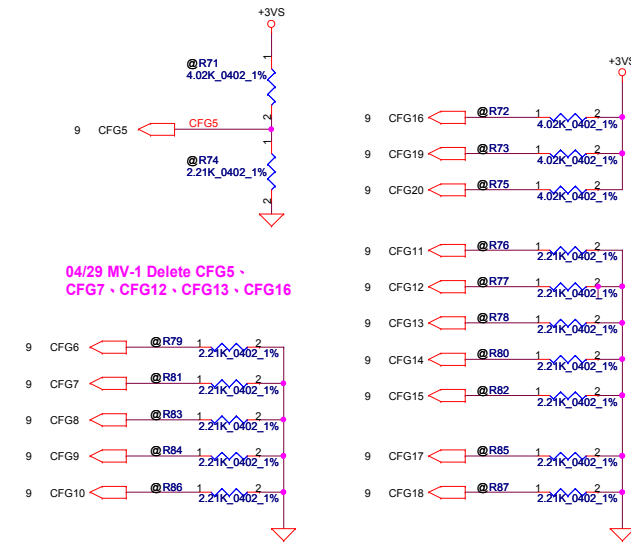
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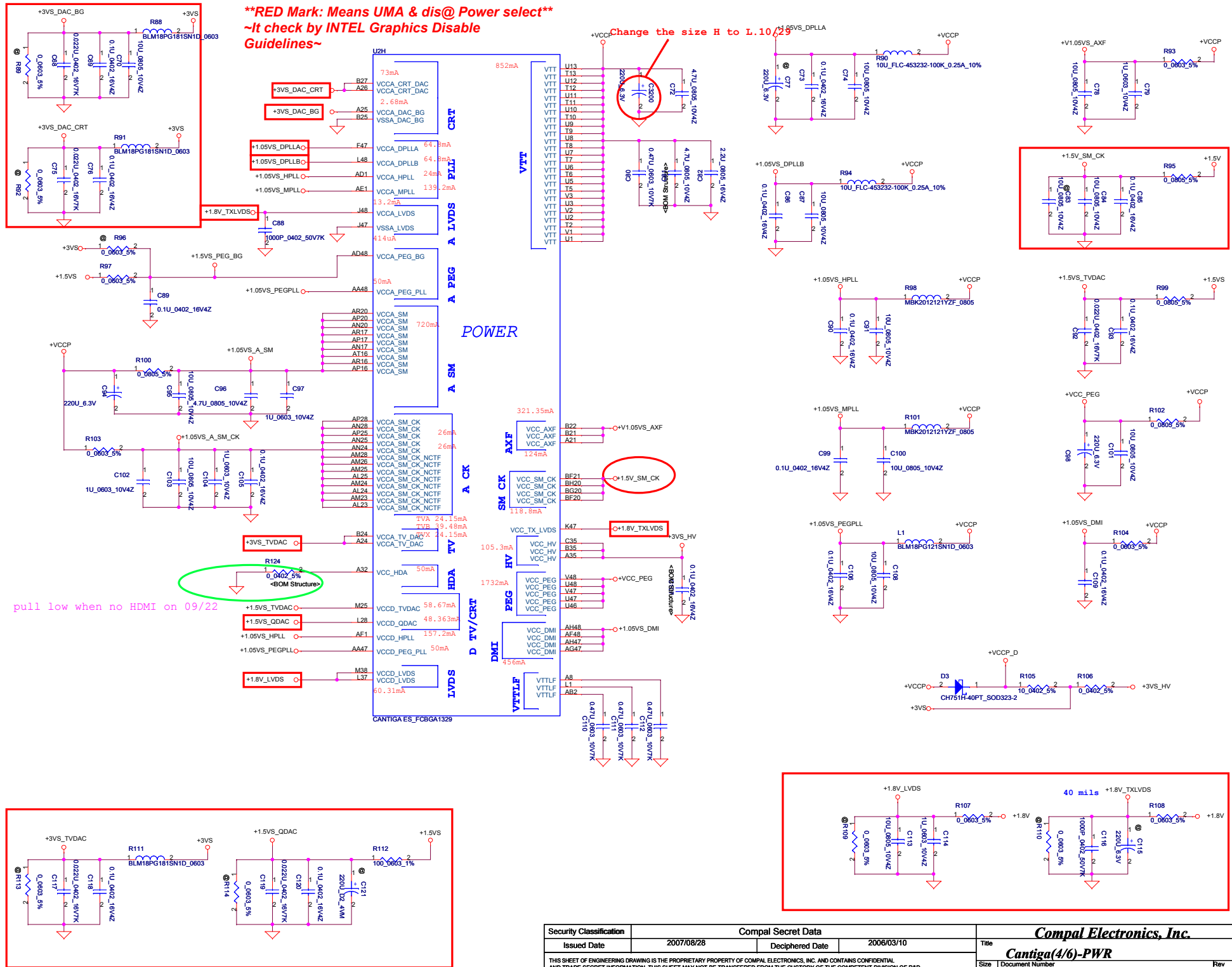
Strap Pin Table

CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The ITPM Host Interface is enable 1 = The ITPM Host Interface is disable *
CFG7 (Intel Management Engine Crypto strap)	0 =(TLS)chiper suite with no confidentiality 1 =(TLS)chiper suite with confidentiality *
CFG8	Reserved
CFG9 (PCIe Graphics Lane Reversal)	0 = Reverse Lane,15->0, 14->1 1 = Normal Operation,Lane Number in order *
CFG10 (PCIe Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation (Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation (Lane number in Order) * 1 = Reverse Lane
CFG20 (PCIe/SDVO concurrent)	0 = Only PCIe or SDVO is operational. * 1 = PCIe/SDVO are operating simu.

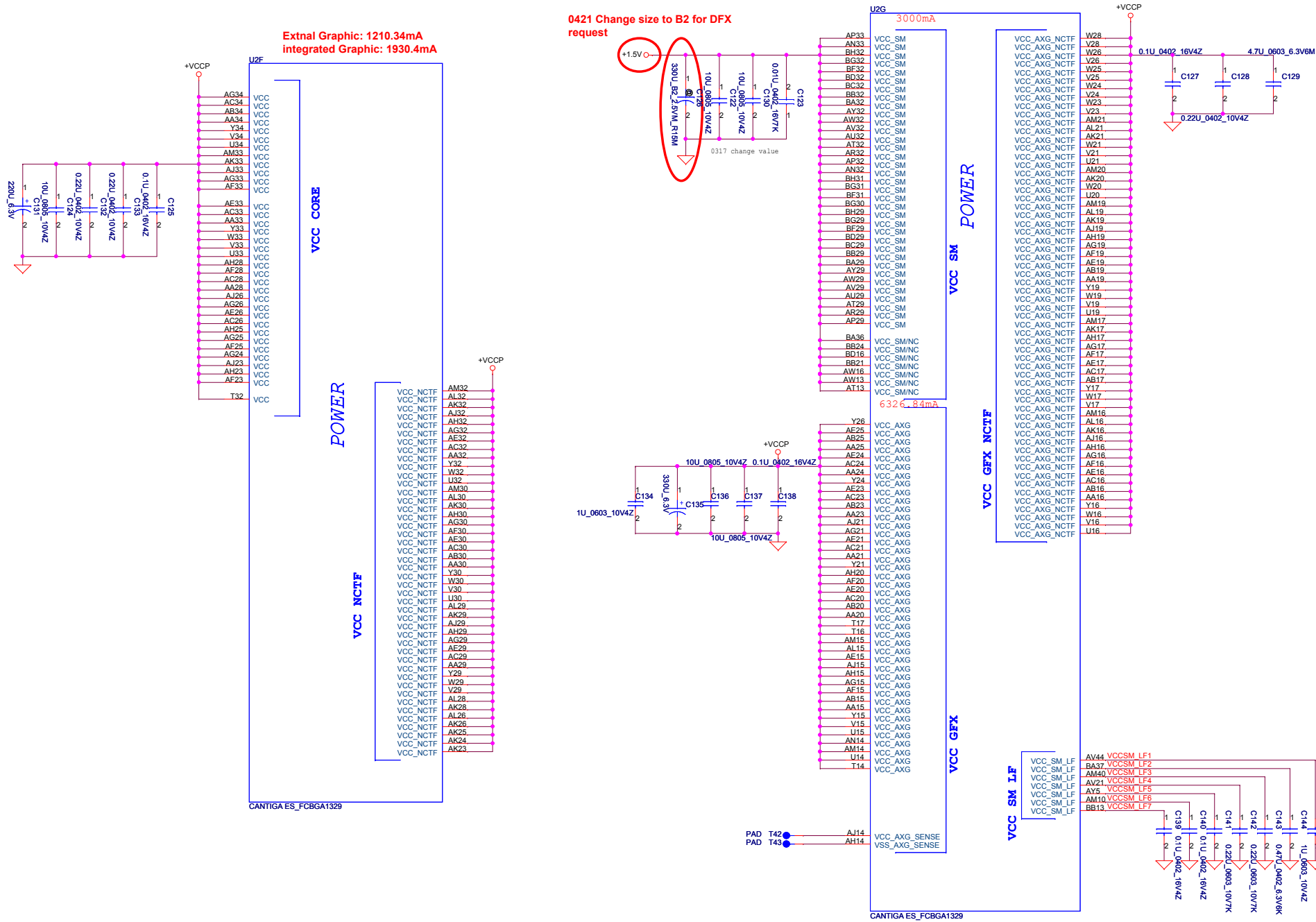


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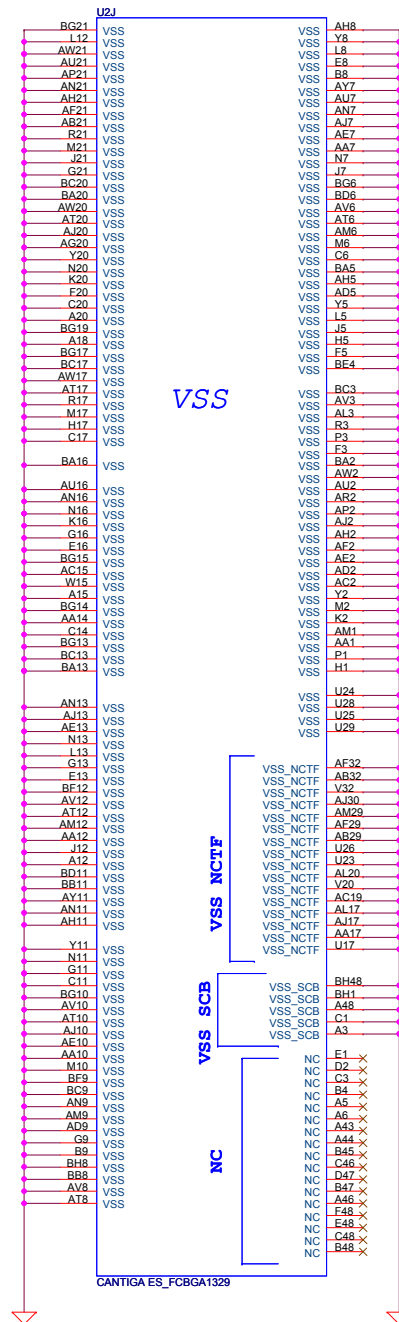
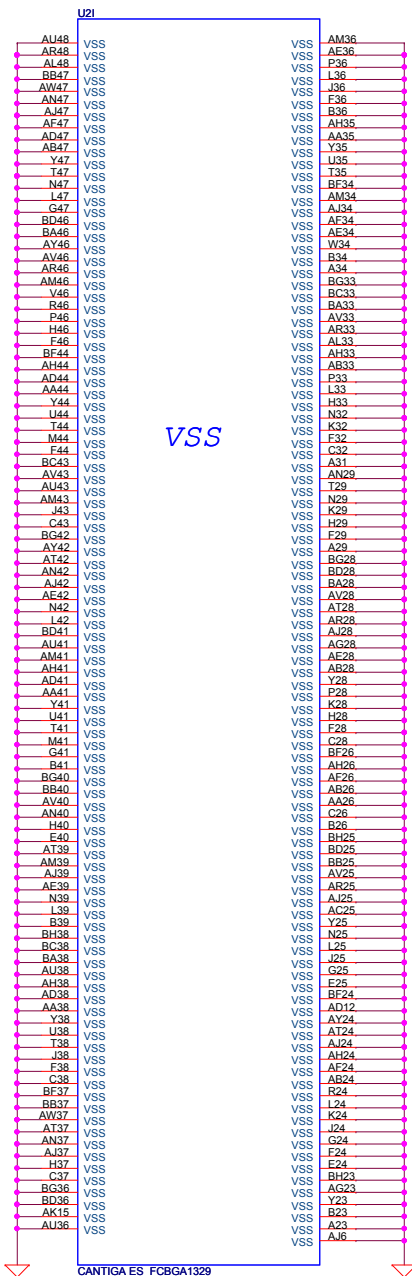
****RED Mark: Means UMA & dis@ Power select****
~It check by INTEL Graphics Disable
Guidelines~



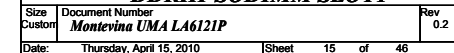
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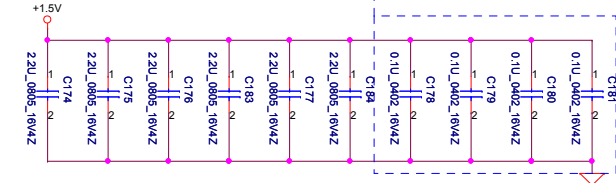
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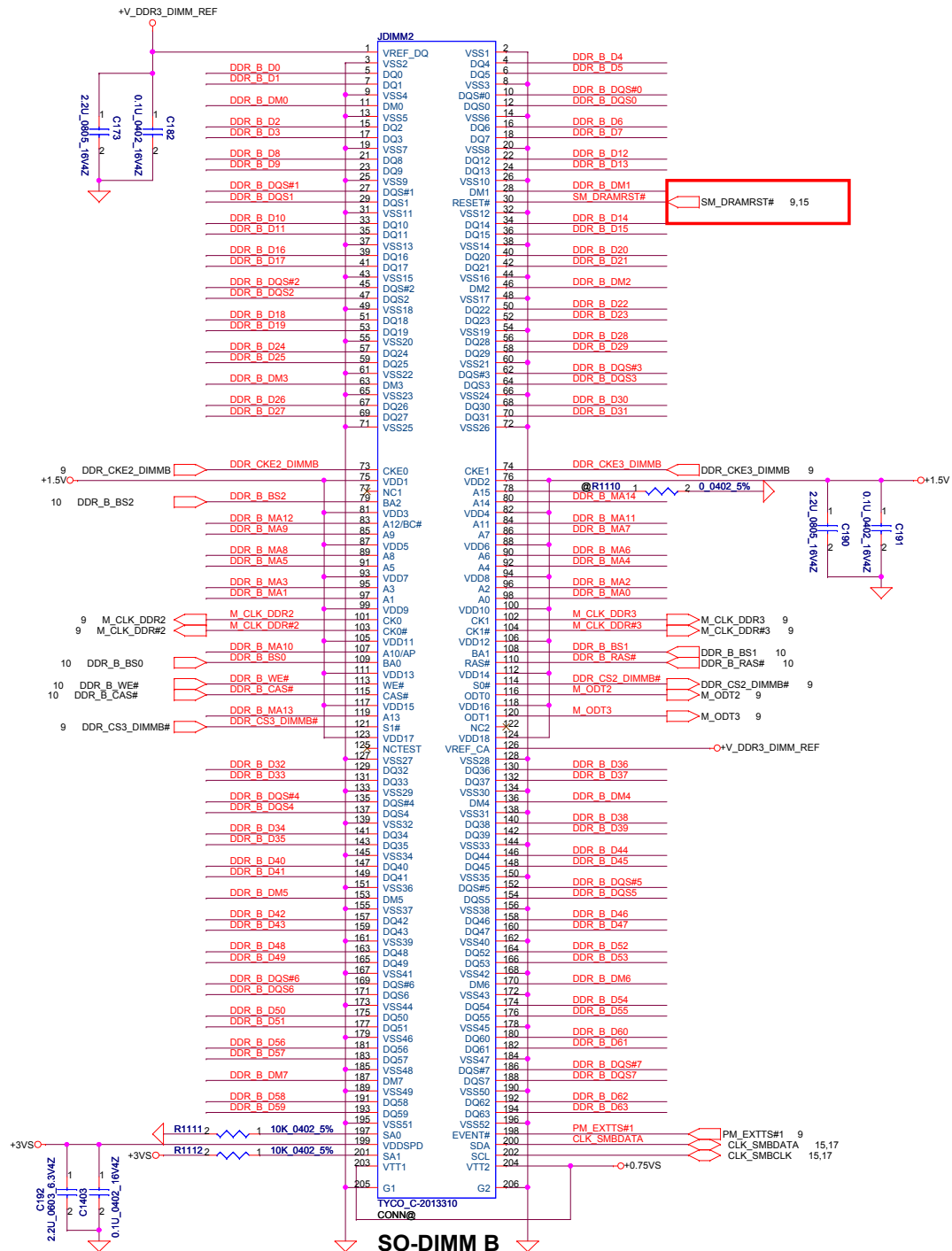
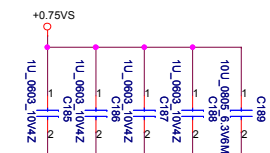
10 DDR_B_DQS#[0..7]
10 DDR_B_D[0..63]
10 DDR_B_DM[0..7]
10 DDR_B_DQS[0..7]
10 DDR_B_MA[0..14]

Layout Note:
Place near
JDIMM2

Layout Note:
Place these 4 caps near Command
and Control signals of DIMMB

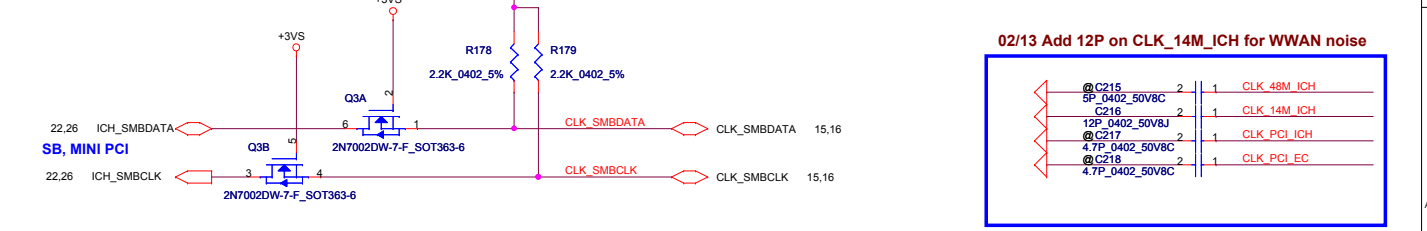
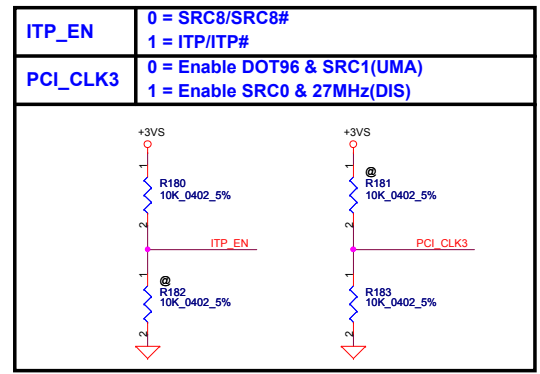
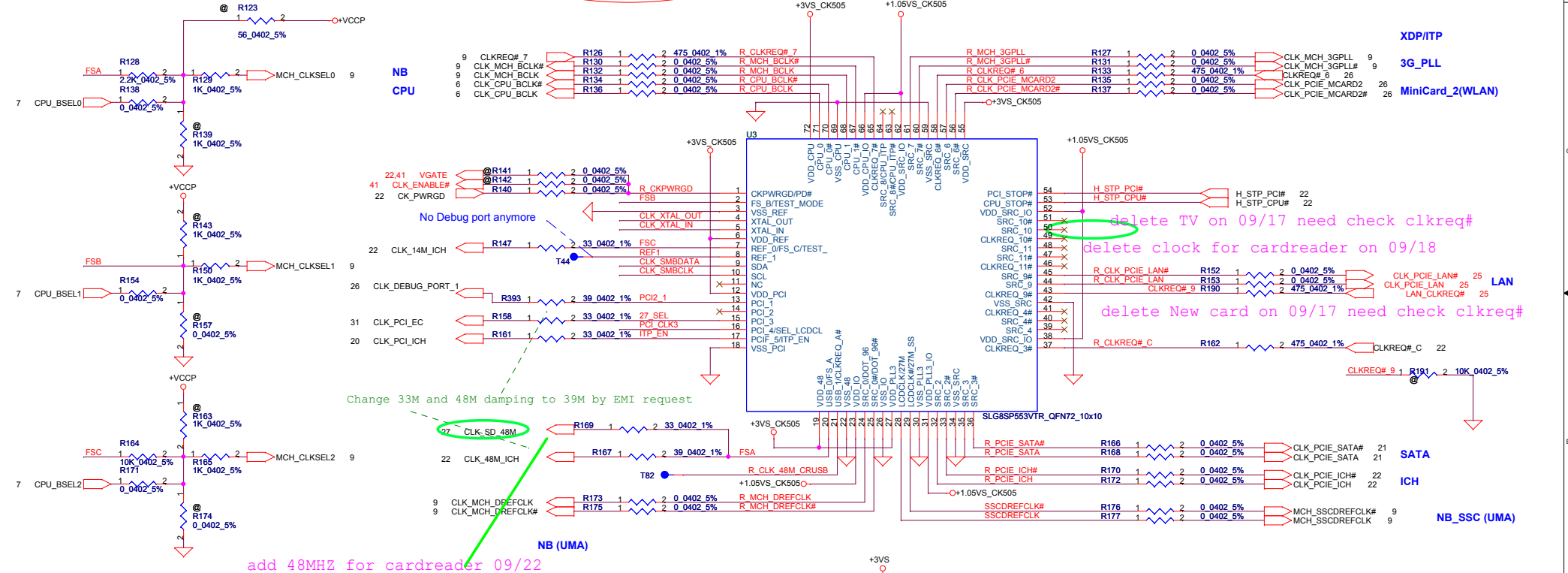
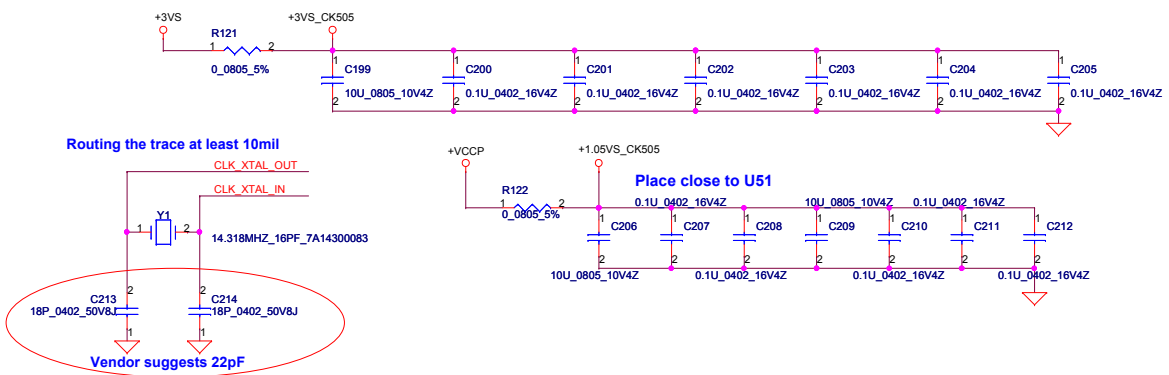


Layout Note:
Place near JDIMM2.203 & JDIMM2.204



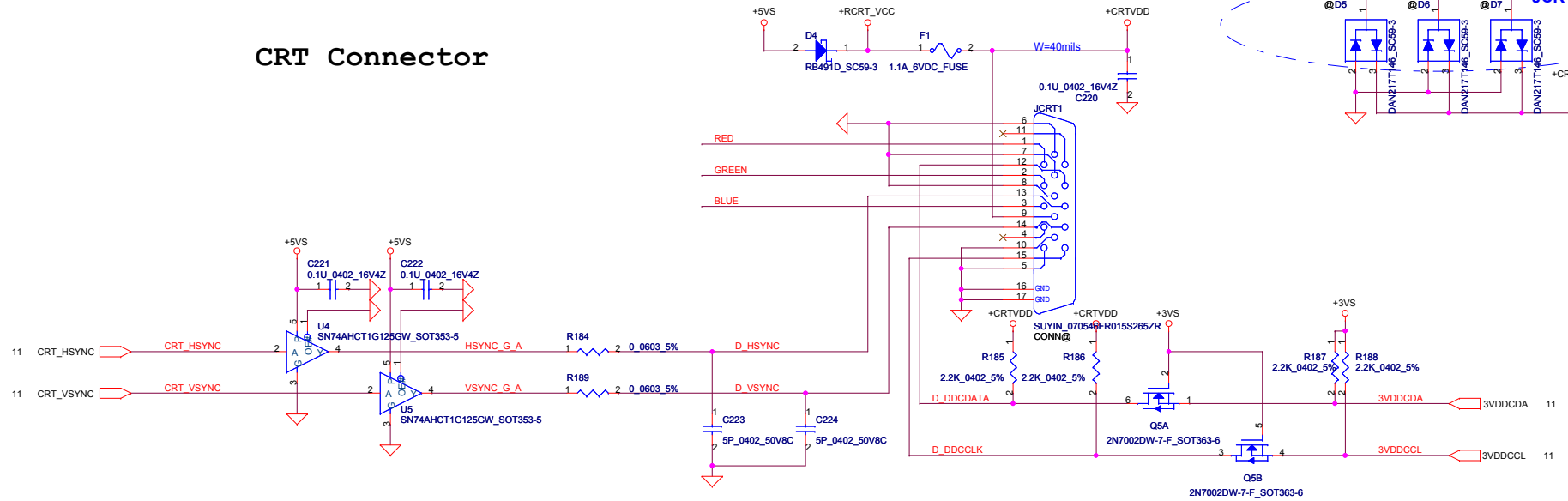
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								DDRIII-SODIMM SLOT2			
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FSC	FSB	FSA	CPU	SRC	PCI	REF	DOT_96	USB
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz	MHz	MHz	MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1						
Reserved								



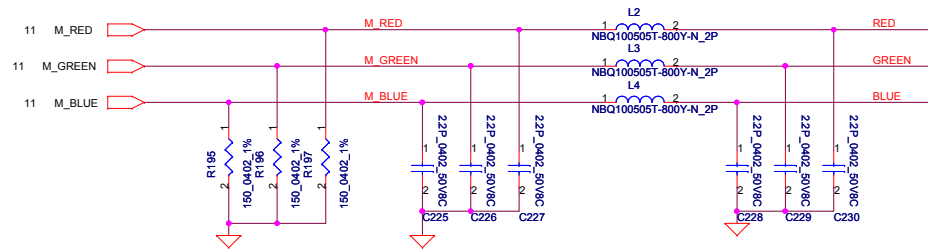
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CRT Connector

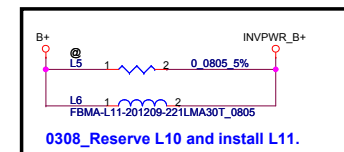
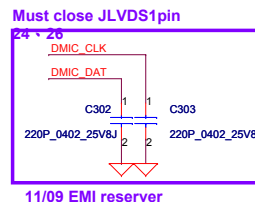
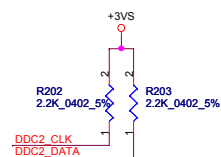
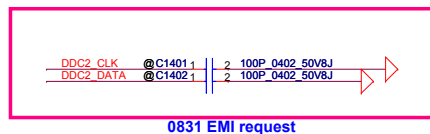
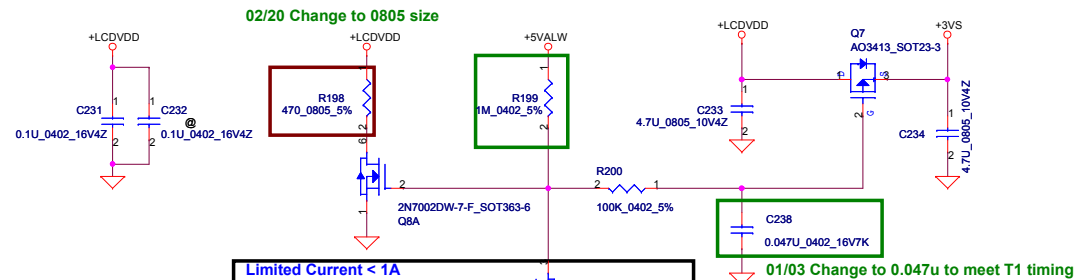
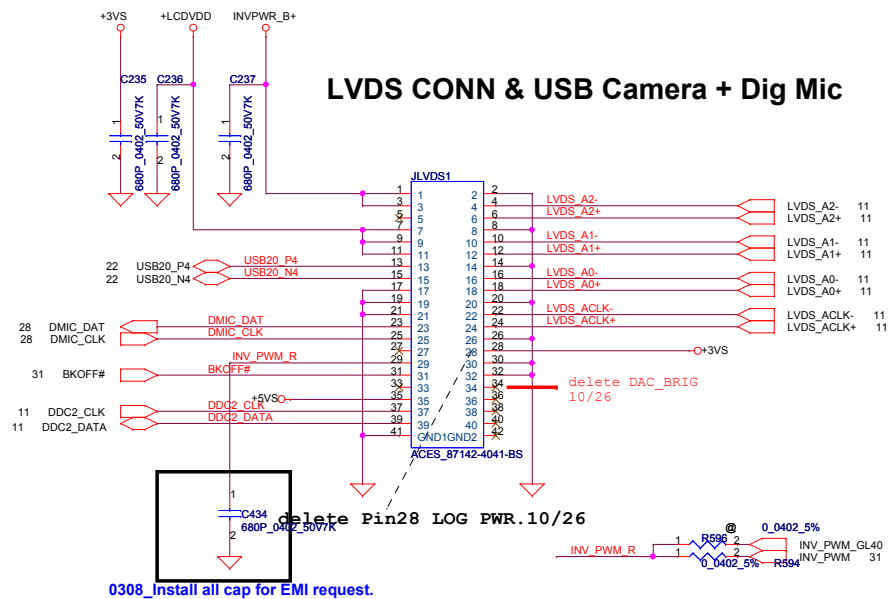


CRT Termination/EMI Filter

11/07 Change CRT louting NB-->Docking-->CRT connector

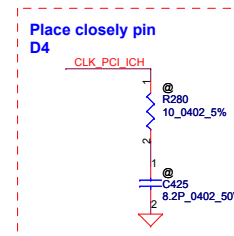
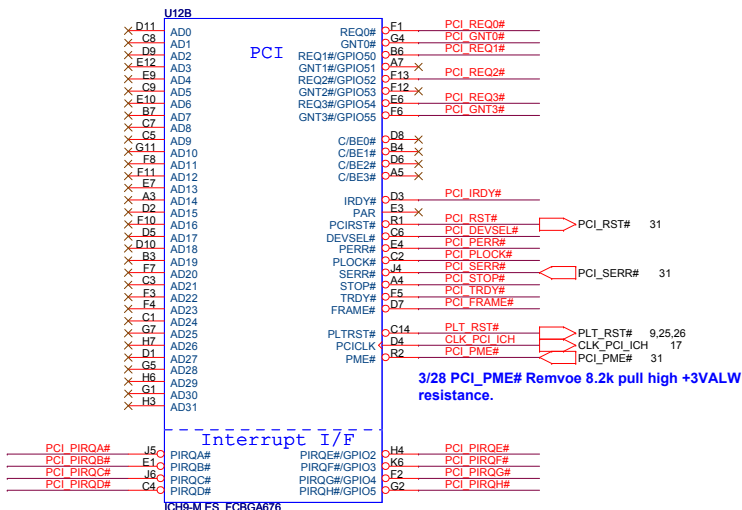
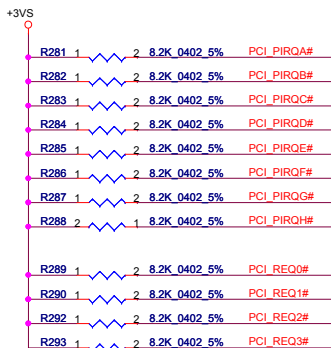
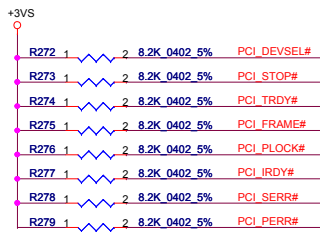


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delete +5VS transfer to +USB_CAM.10/26

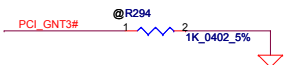
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Delete GS function

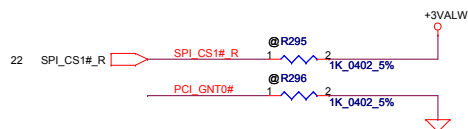
A16 swap override Strap

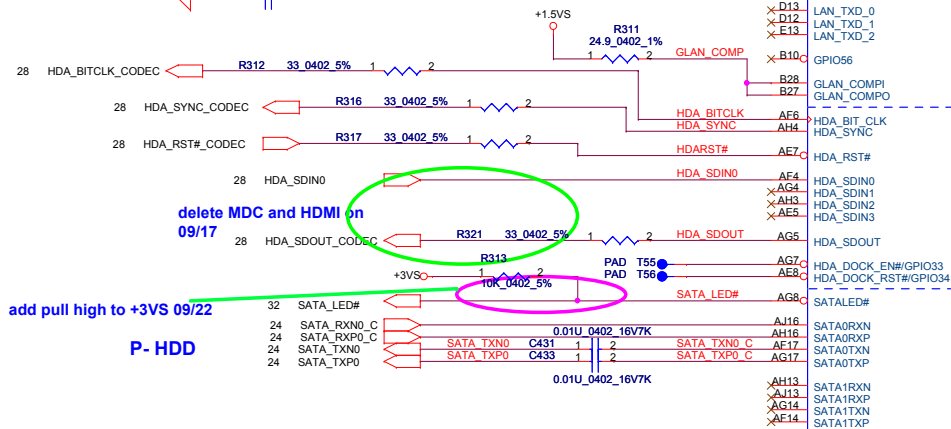
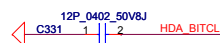
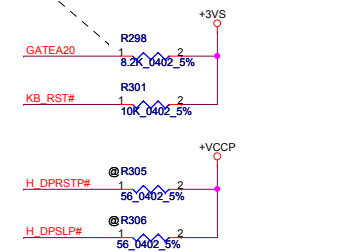
PCI_GNT3#	Low= A16 swap override Enable
	High= *
	Default



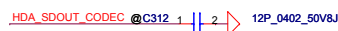
Boot BIOS Strap

PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *

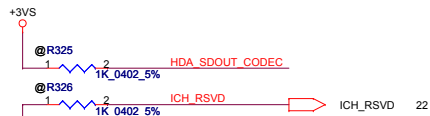




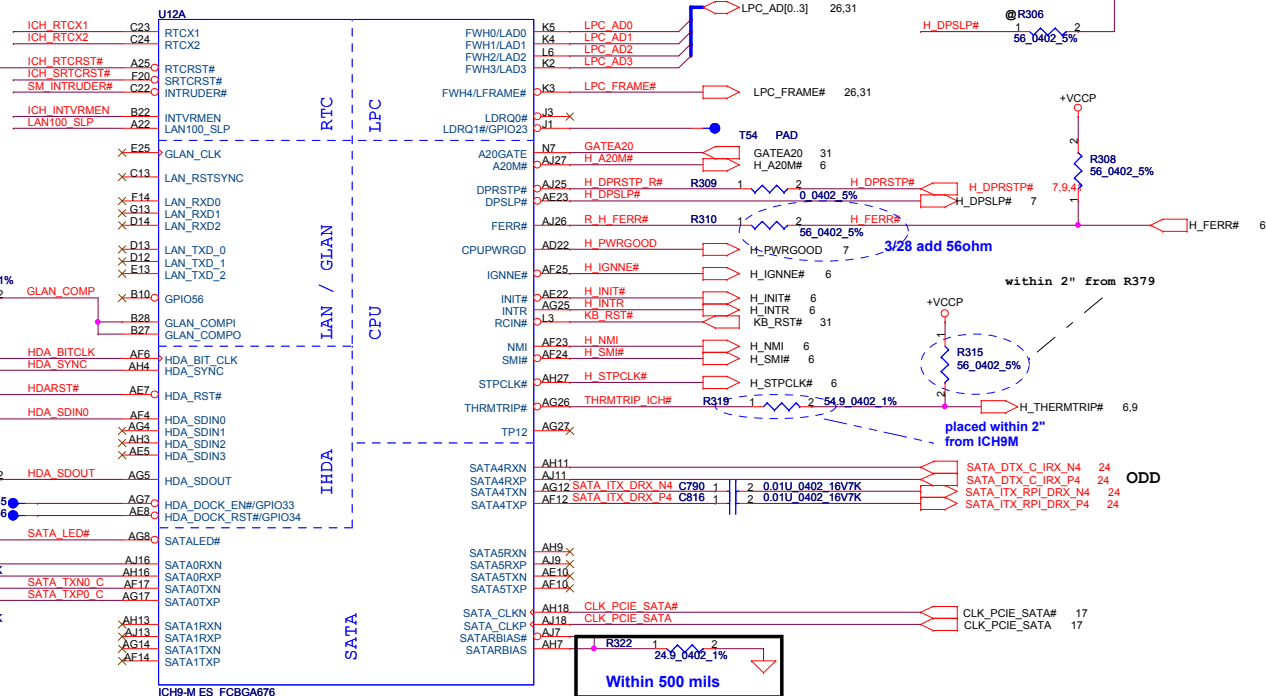
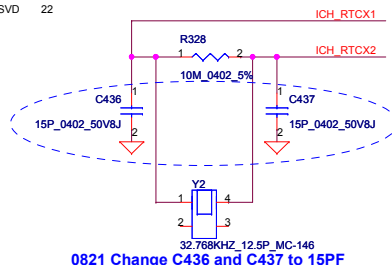
Add 12p on HDA_SDOUT and HDA_SDOUT



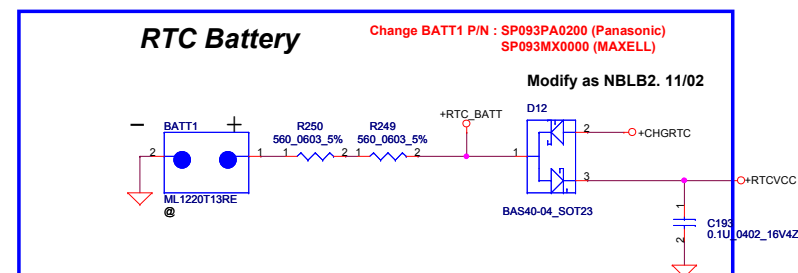
XOR CHAIN ENTRANCE STRAP:RSVD



ICH_RSVD	HDA_SDOUT_CODEC	
0	0	
0	1	
1	0	
1	1	

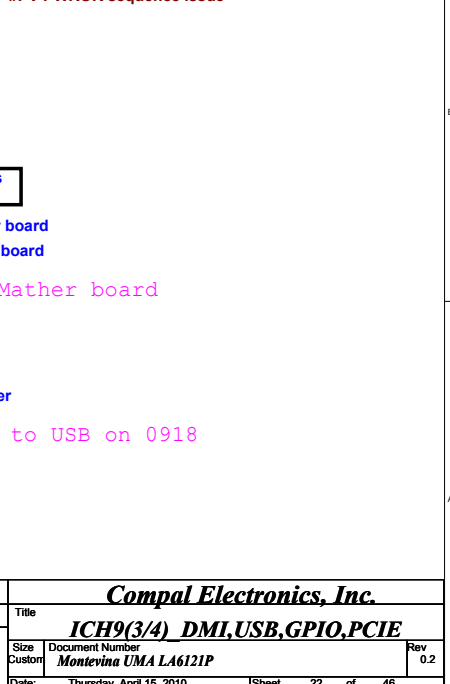
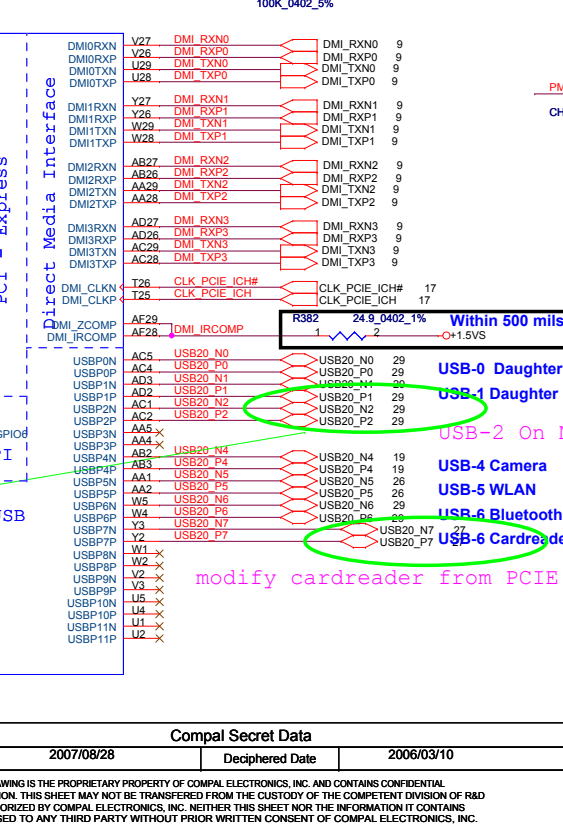
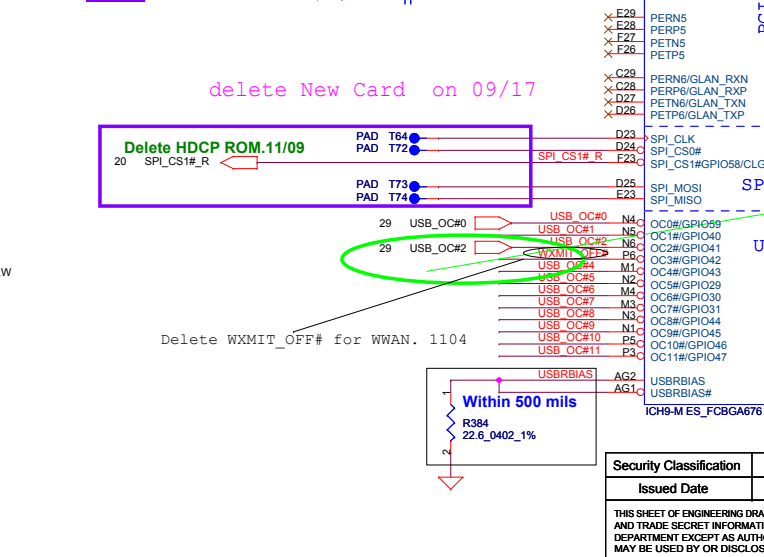
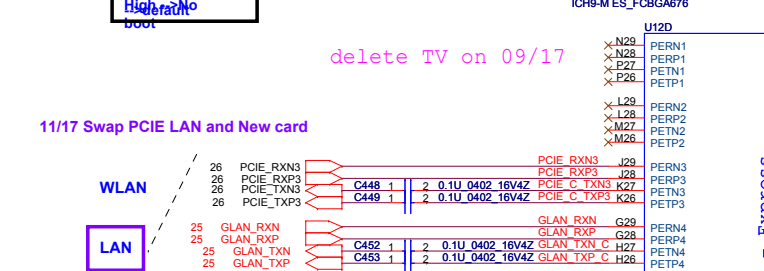


02/13 Reserve cap on HDA_BITCLK for WWAN noise issue



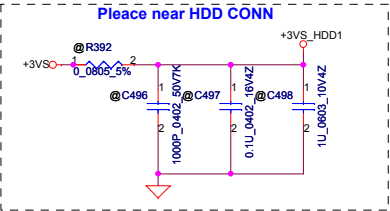
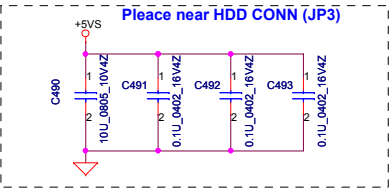
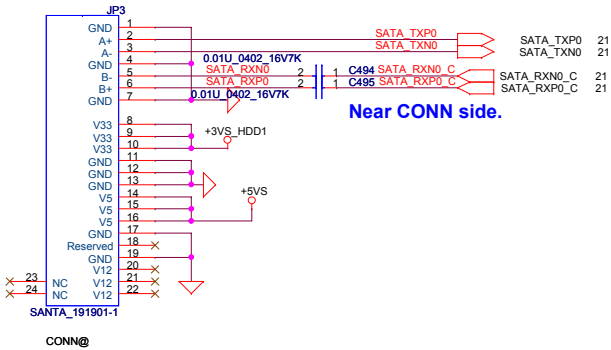
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2007/08/28	Deciphered Date	2006/03/10	Title	ICH9(2/4) LAN,HD,IDE,LPC
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				Document Number	0.2
				Montevina UA L6121P	
Date:	Thursday, April 15, 2010	Sheet	21	of	46

Pin configuration diagram for the R333 pin header. The diagram shows a 3V3 power supply connected to pin 1. Pins 2 through 19 are configured for various functions: SIRQ, PM_CLKRUN#, OCP#, THERM_SC#, CLKREQ#_C, PM_BMBUSY#, EC_SC#, GPIO6, GPIO22, GPIO18, GPIO19, GPIO20, GPIO21, GPIO36, GPIO37, GPIO39, GPIO48, and GPIO57. Each pin is labeled with its number, a 10K pull-up resistor, and a 0402 5% resistor. The diagram also shows a +1.7V ADD R337 clock REQ pull high connection.

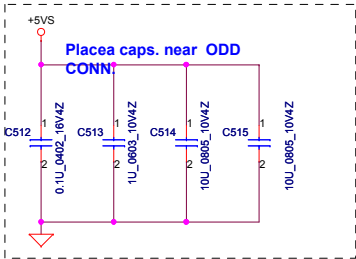
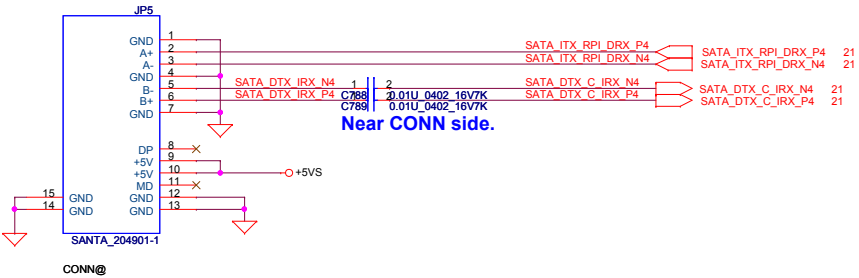


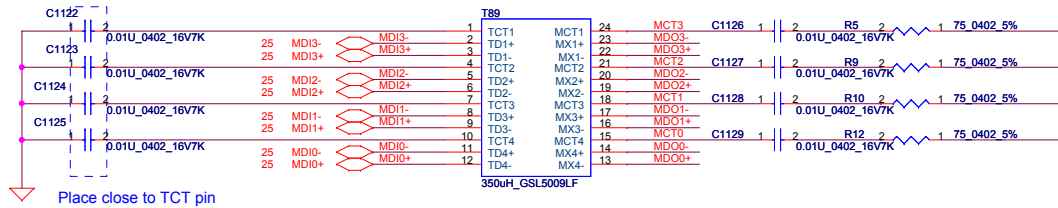
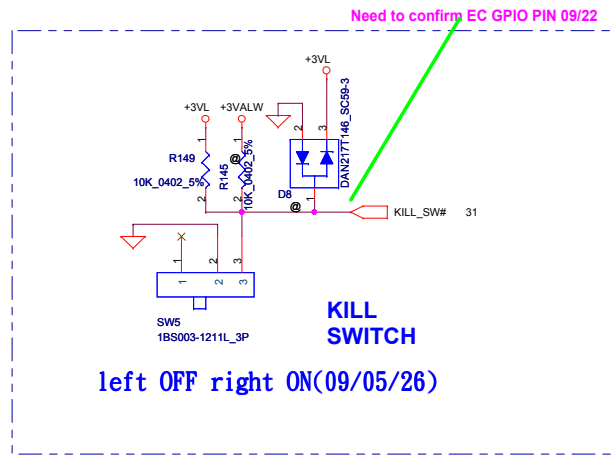
Security Classification		Compal Secret Data		Compal Electronics, Inc. ICH9(3/4) DMI,USB,GPIO,PCIE	
Issued Date	2007/08/28	Deciphered Date	2006/03/10	Title	
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				Custom	Montevina UMA L46121P
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HDD Connector



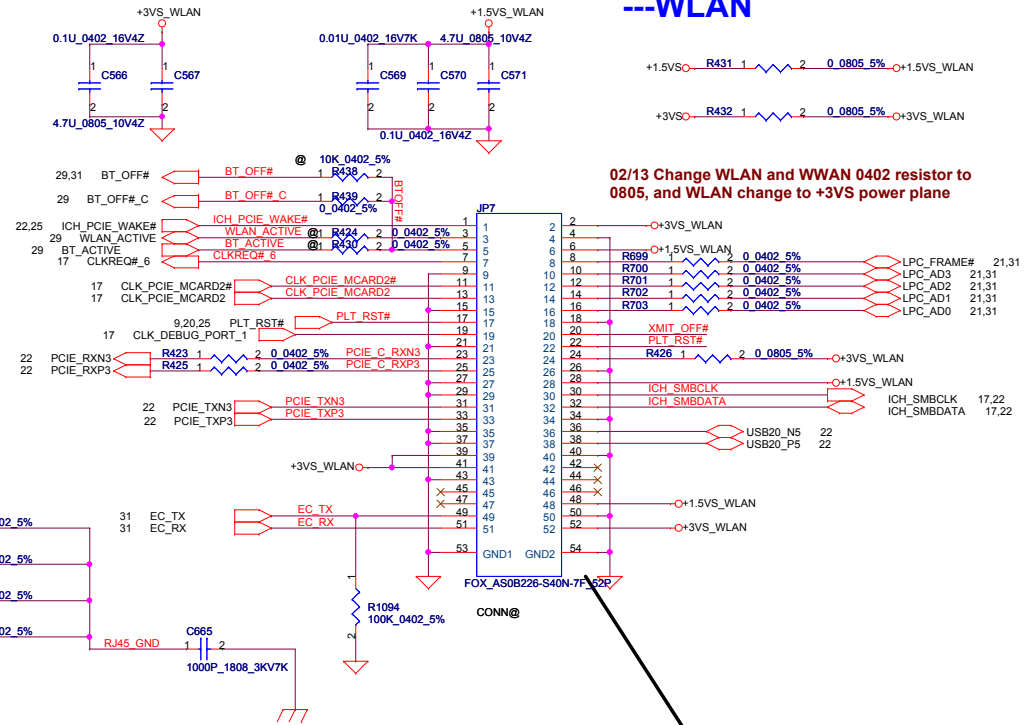
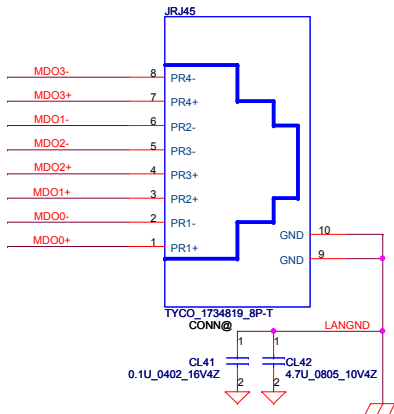
CD-ROM Connector





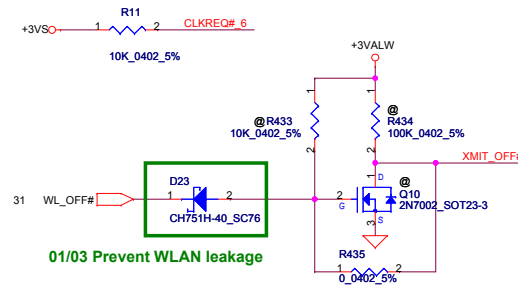
Modify as B3B5. 11/11

LAN Conn.



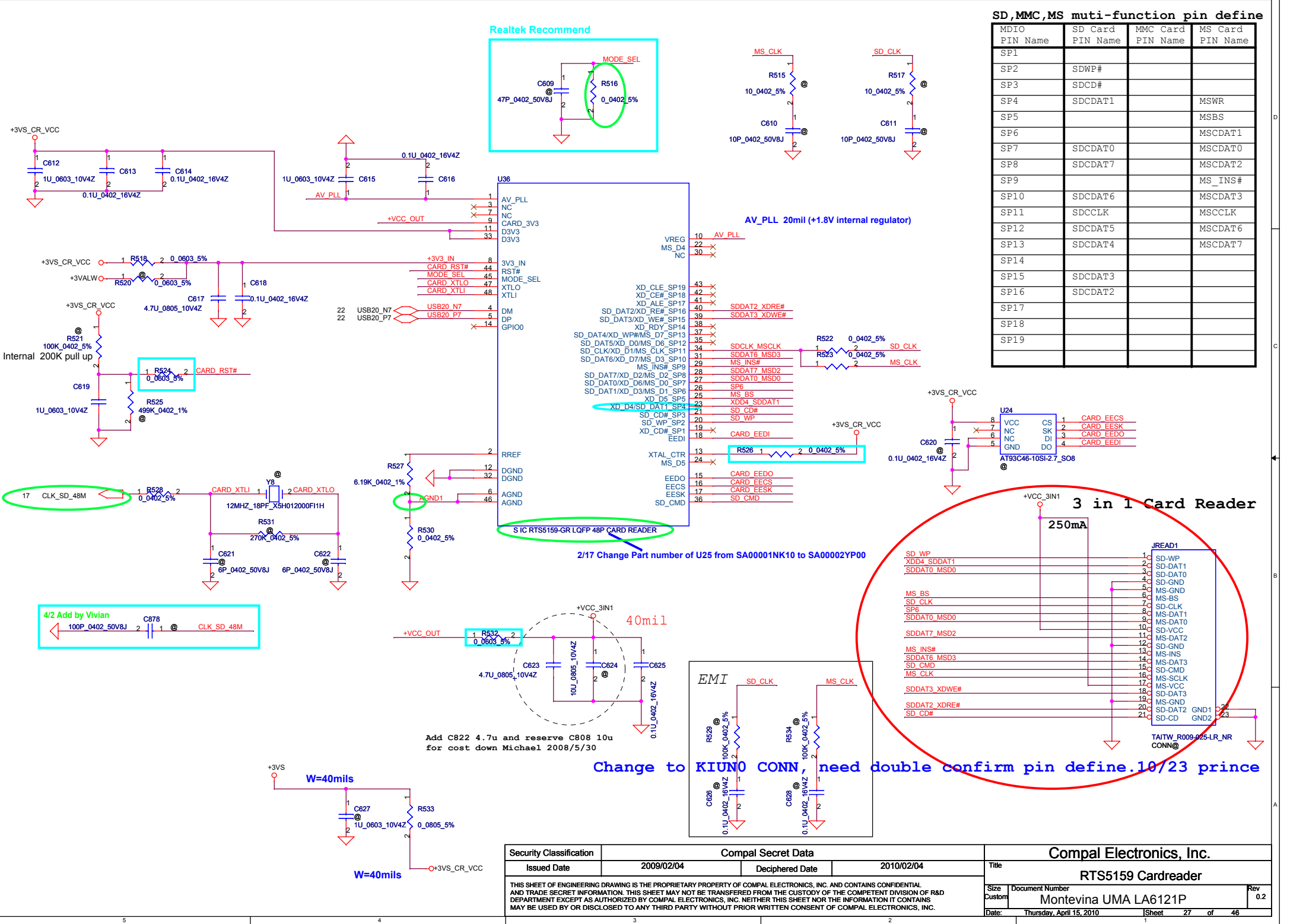
Change to IAT50 footprint, because of error layout symbol. 1202

04/29 MV-1 add clock REQ pull high



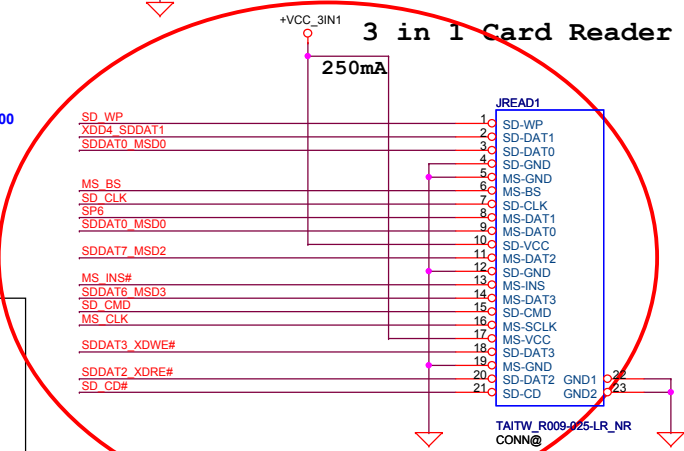
01/03 Prevent WLAN leakage

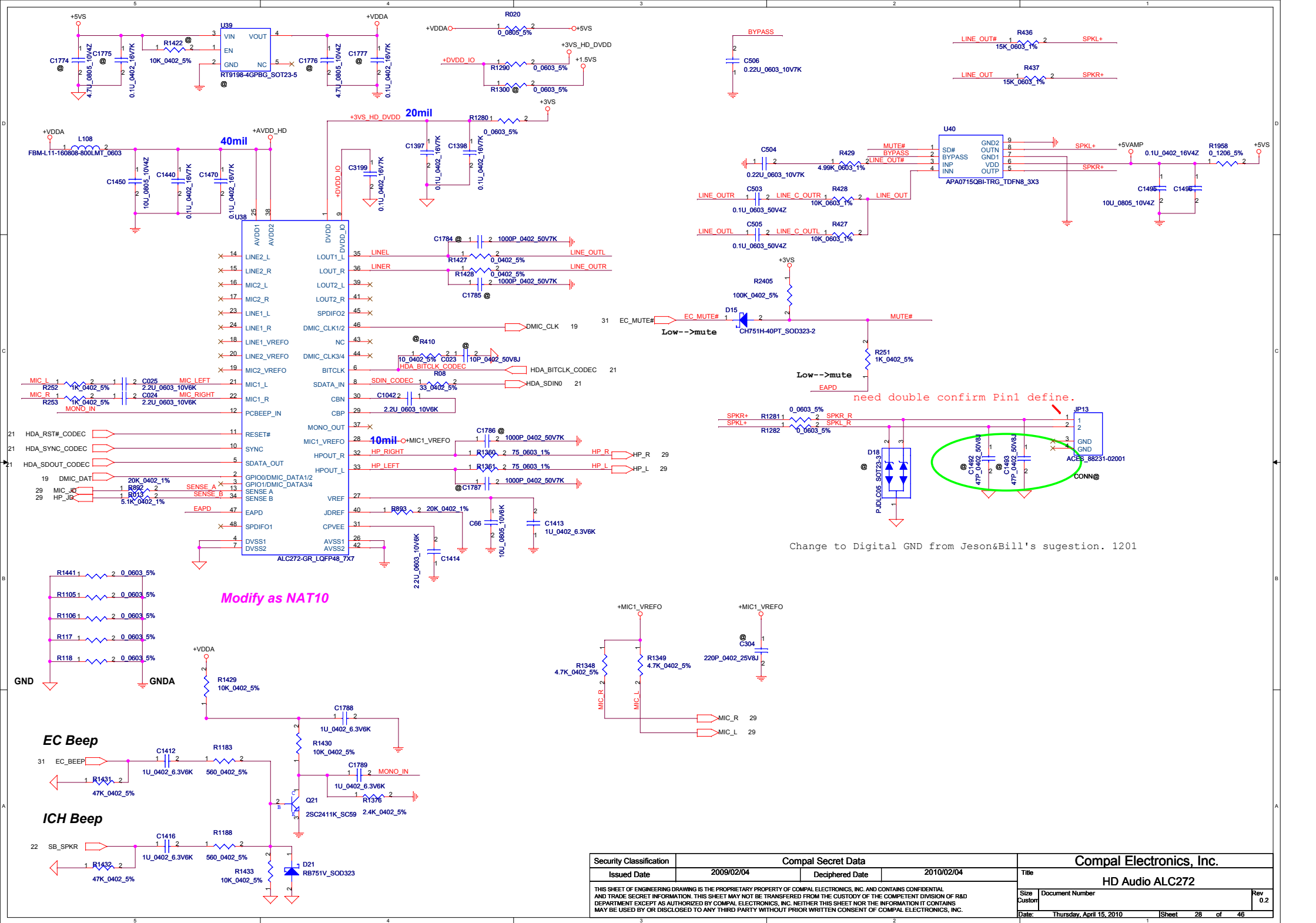
Security Classification		Compal Secret Data		Compal Electronics, Inc.			
Issued Date		2007/08/28	Deciphered Date	2006/07/26	Title		
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					Size	Document Number	Rev
						Montevina UMA LA6121P	0.2
Date:		Thursday, April 15, 2010		Sheet	26	of 46	

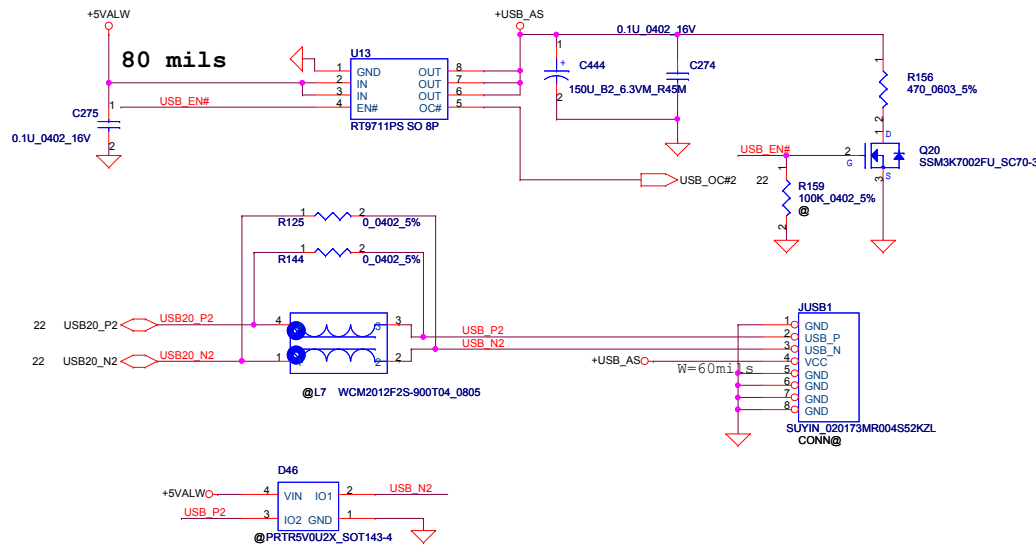


SD,MMC,MS muti-function pin define

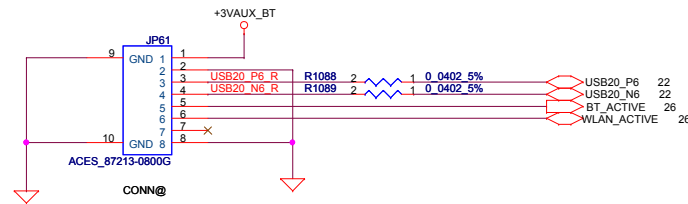
MDIO PIN Name	SD Card PIN Name	MMC Card PIN Name	MS Card PIN Name
SP1			
SP2	SDWP#		
SP3	SDCD#		
SP4	SDCDAT1		MSWR
SP5			MSBS
SP6			MSCDAT1
SP7	SDCDAT0		MSCDAT0
SP8	SDCDAT7		MSCDAT2
SP9			MS_INS#
SP10	SDCDAT6		MSCDAT3
SP11	SDCLK		MSCCLK
SP12	SDCDAT5		MSCDAT6
SP13	SDCDAT4		MSCDAT7
SP14			
SP15	SDCDAT3		
SP16	SDCDAT2		
SP17			
SP18			
SP19			



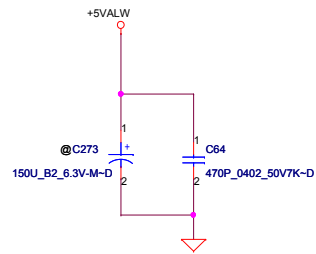




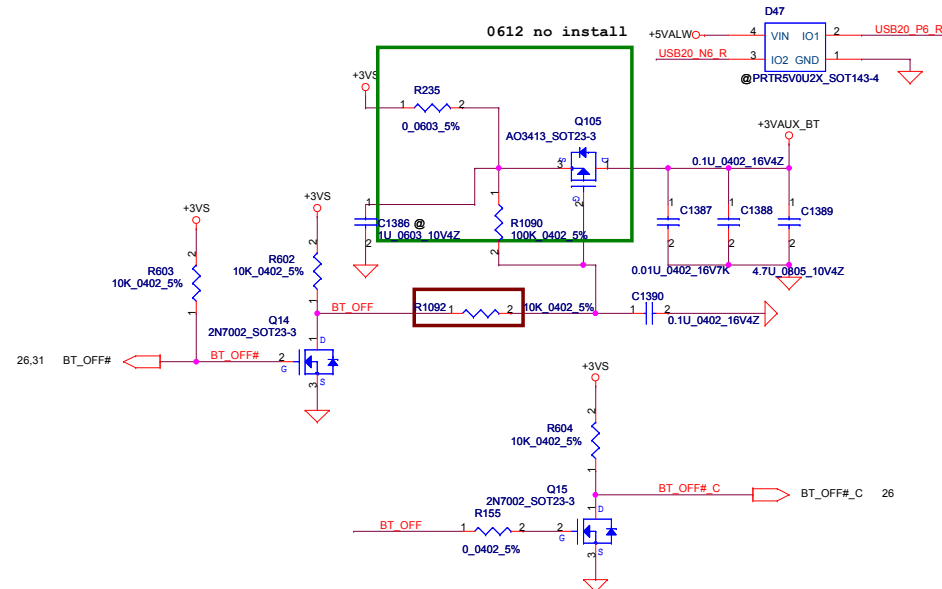
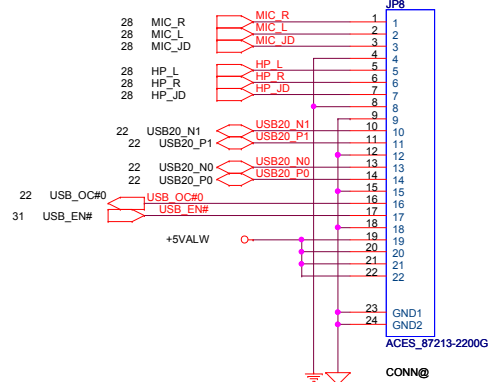
BT Connector



modify on 09/17 and need to confirm with ME

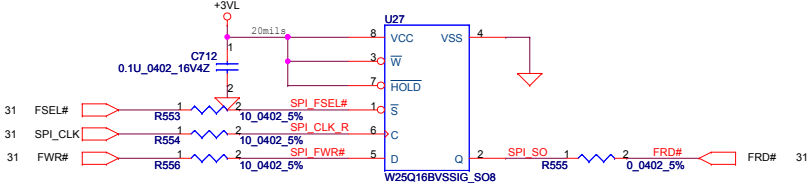


USB/B to M/B Conn.

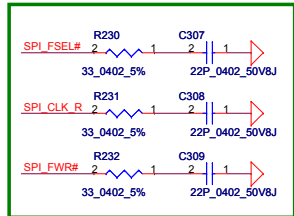


Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2007/08/28				Title			
				Deciphered Date				2006/07/26			
								USB, BT, eSATA			
								Montevina UMA LA6121P			
								Rev 0.2			
								Date: Thursday, April 15, 2010			
								Sheet 29 of 46			

SPI ROM



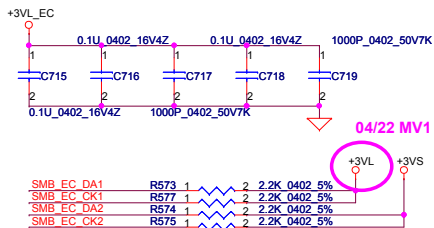
SP07000F500 S SOCKET WIESON G6179-100000 8P
SPIFLASH
WIESO_G6179-100000_8P



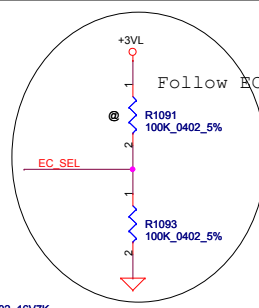
12/27EMI
request

Remove LPC Debug Port
20090618

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				Size	Document Number	Rev
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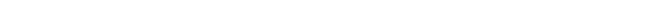
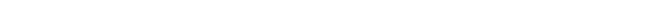
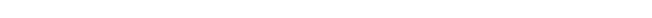
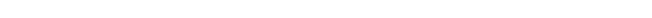
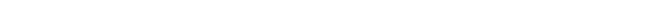
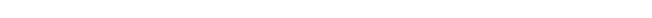
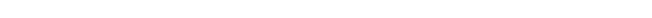
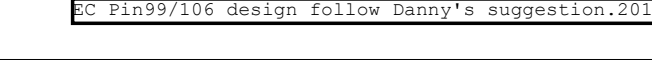
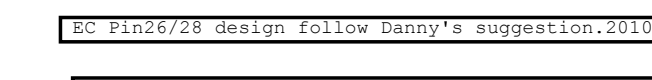
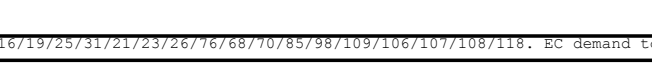
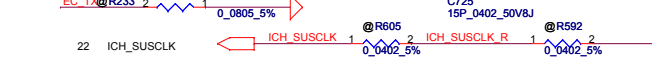
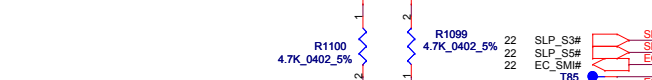
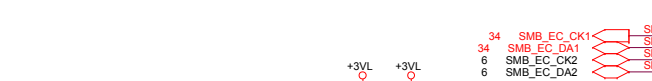
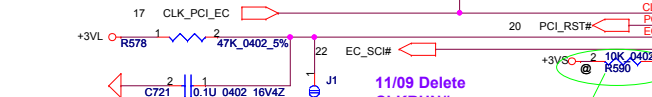
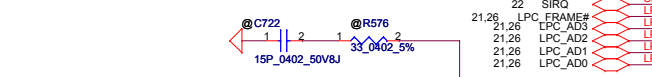
EC_SEL	EC_VERSION
High	KB926D3
Low	KB926E0



Follow EC's request.01/18

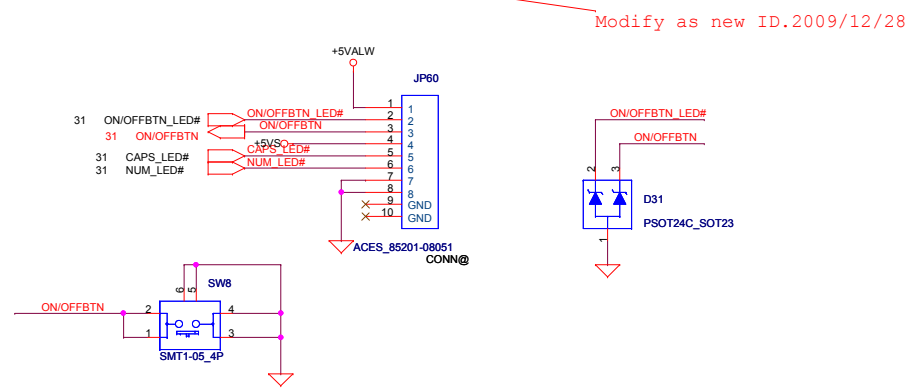
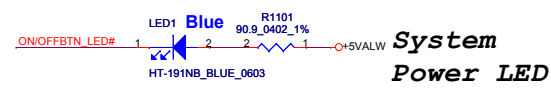
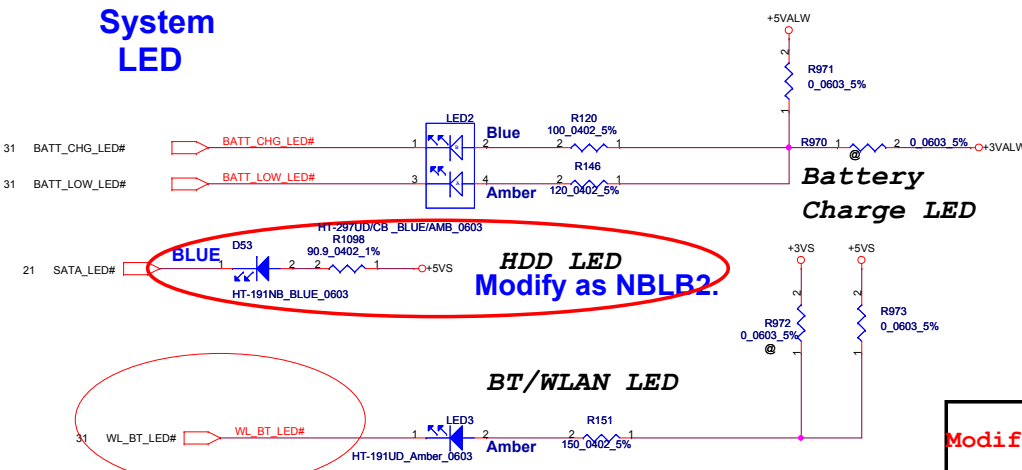
For EMI

03/28 PV2 Change SM bus power to +3VL



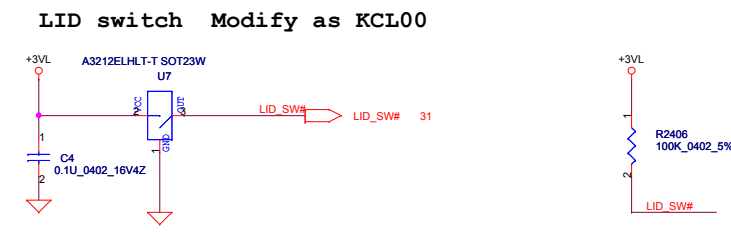
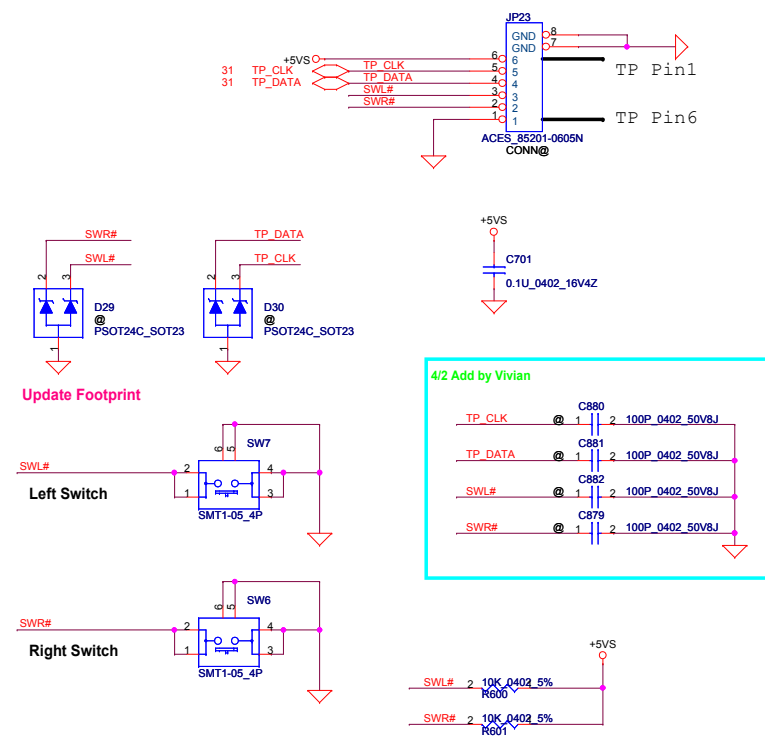
Need to confirm LED coulor

System LED



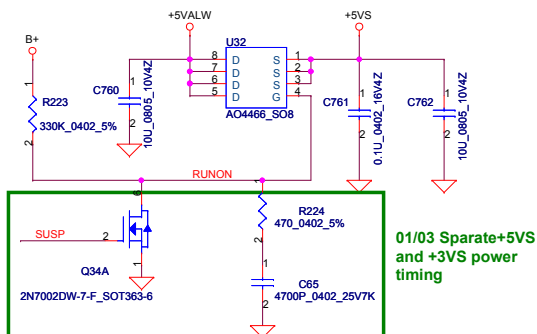
Modify as NBLB2, need double confirm CONN pin define. 10/24 Prince

To TP/B Conn.

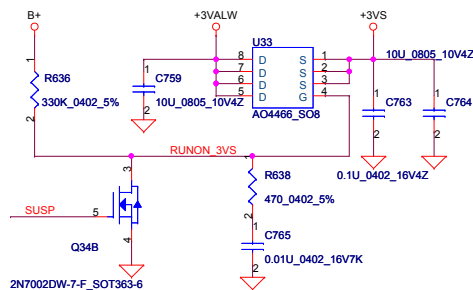


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				Montevina UMA LA6121P	Rev 0.2
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+5VALW to +5VS Transfer



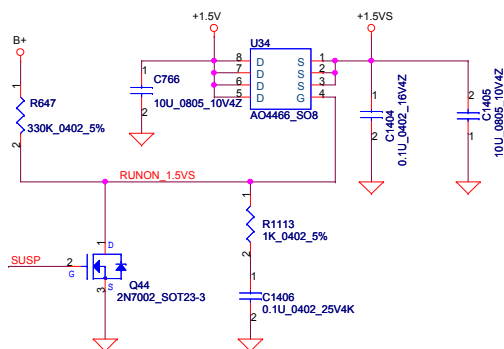
+3VALW to +3VS Transfer



DEL DIM LED 9/30 Prince

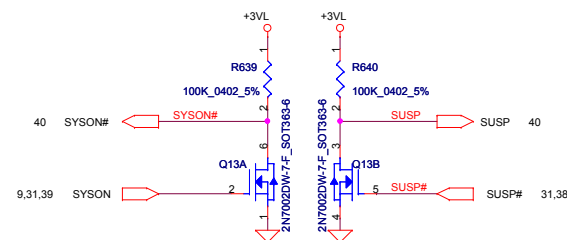
DIM LED

+1.5V to +1.5VS Transfer

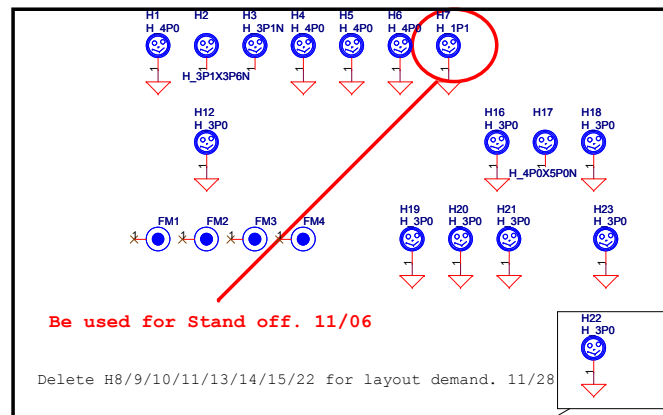
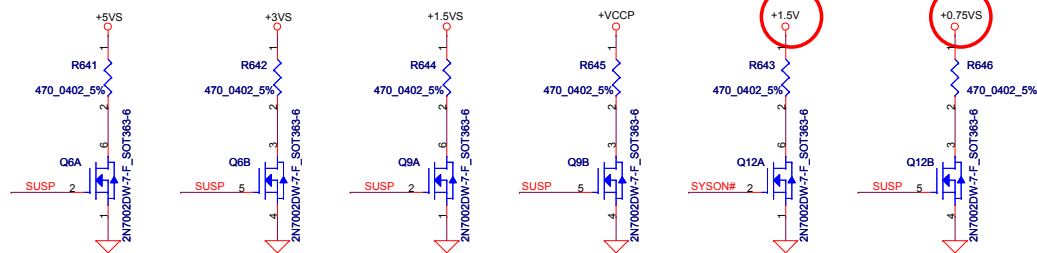


$$V_{OUT} = 1.25(1 + R_{912}/R_{913})$$

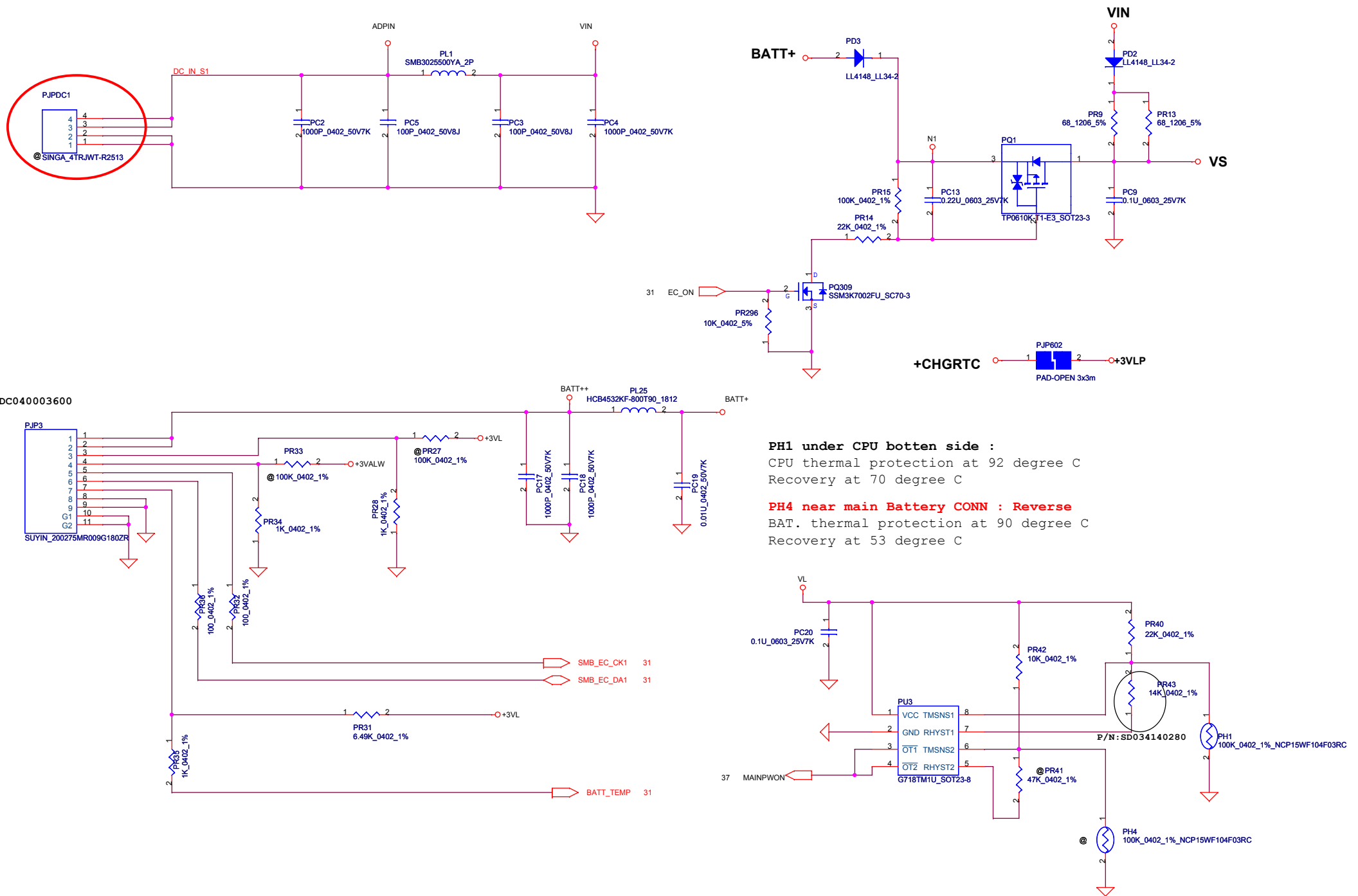
$$V_{OUT} = 1.25(1 + 100k/215k) = 1.83V$$



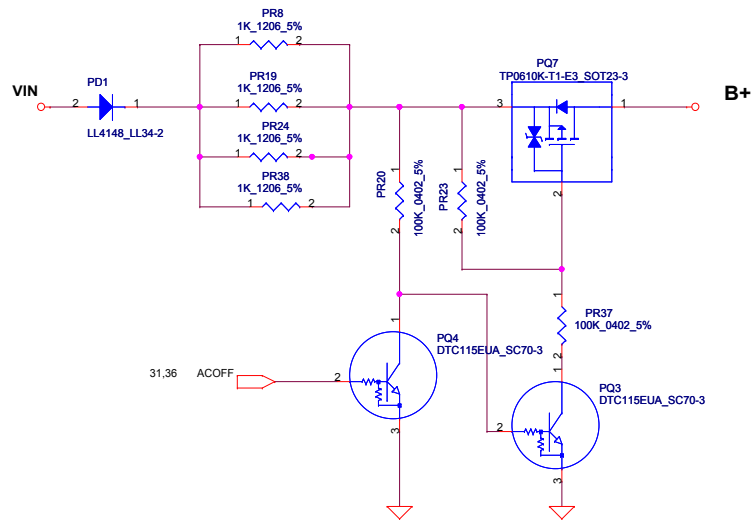
Discharge circuit



Security Classification		Compal Secret Data		Title	
Issued Date	2007/08/28	Deciphered Date	2006/07/26	DC/DC Interface	
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				Montevina UMA LA6121P	
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Security Classification		Compal Secret Data		Title	
Issued Date	2007/05/29	Deciphered Date	2008/05/29	DC Connector/CPU OTP	
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				Montevina Blade UMA LA4105P	
				Date:	Thursday, April 15, 2010
				Sheet	34 of 46
				Rev	1.0



ACIN

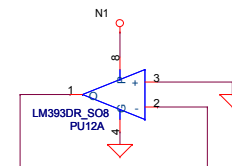
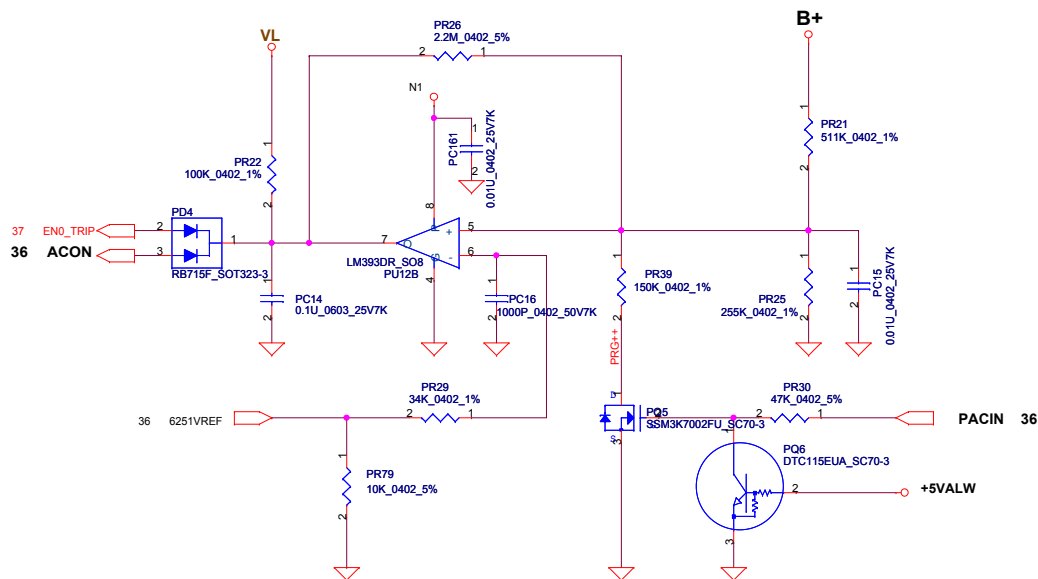
Precharge detector

	Min.	typ.	Max.
H->L	14.589V	14.84V	15.243V
L->H	15.562V	15.97V	16.388V

BATT ONLY

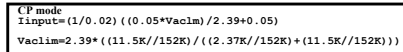
Precharge detector

	Min.	typ.	Max.
H->L	6.138V	6.214V	6.359V
L->H	7.196V	7.349V	7.505V



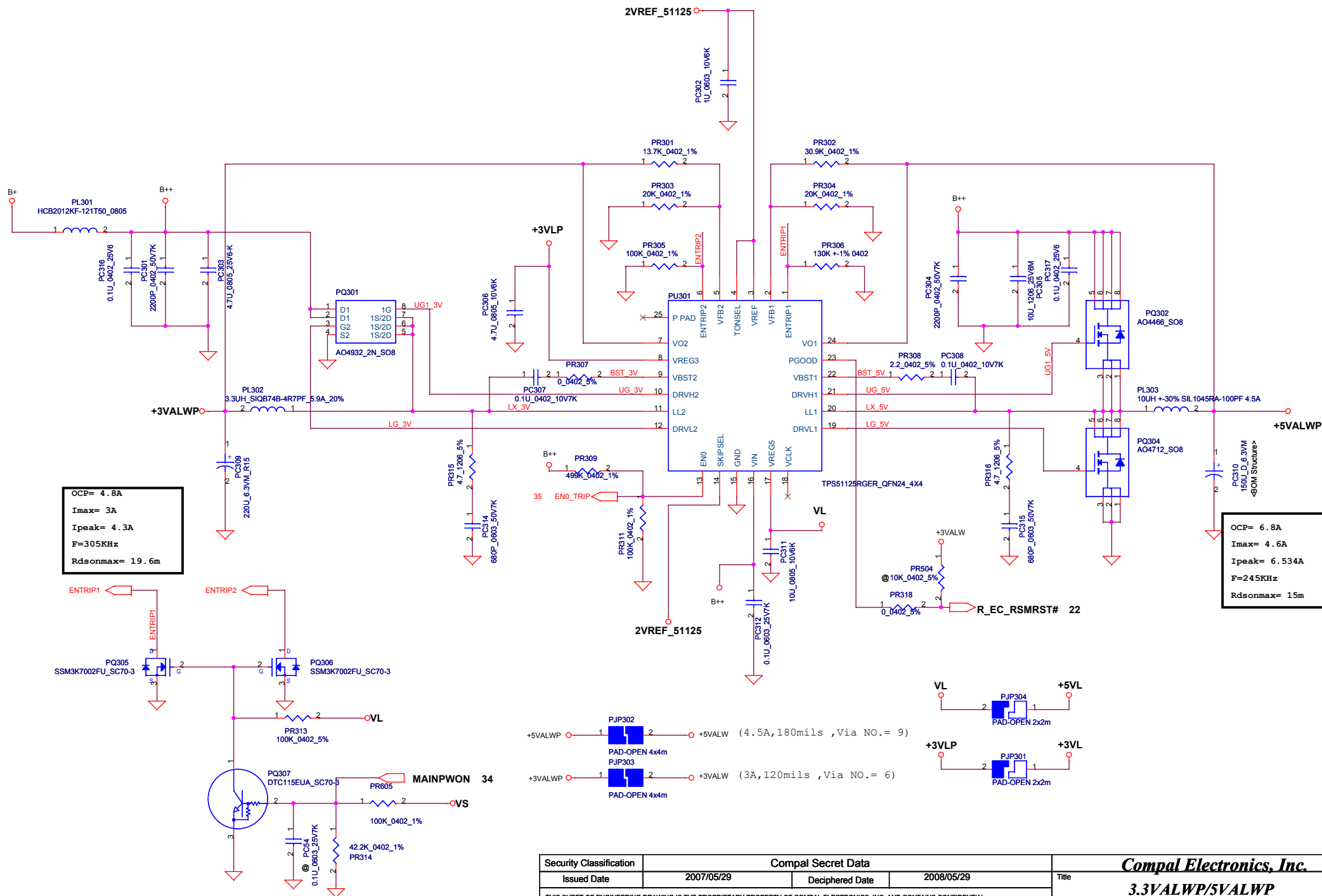
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Issued Date	2009/2/6	Deciphered Date	2010/2/6	Title	
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CP = 85%*Iada (Acer criteria); CP = 2.95A



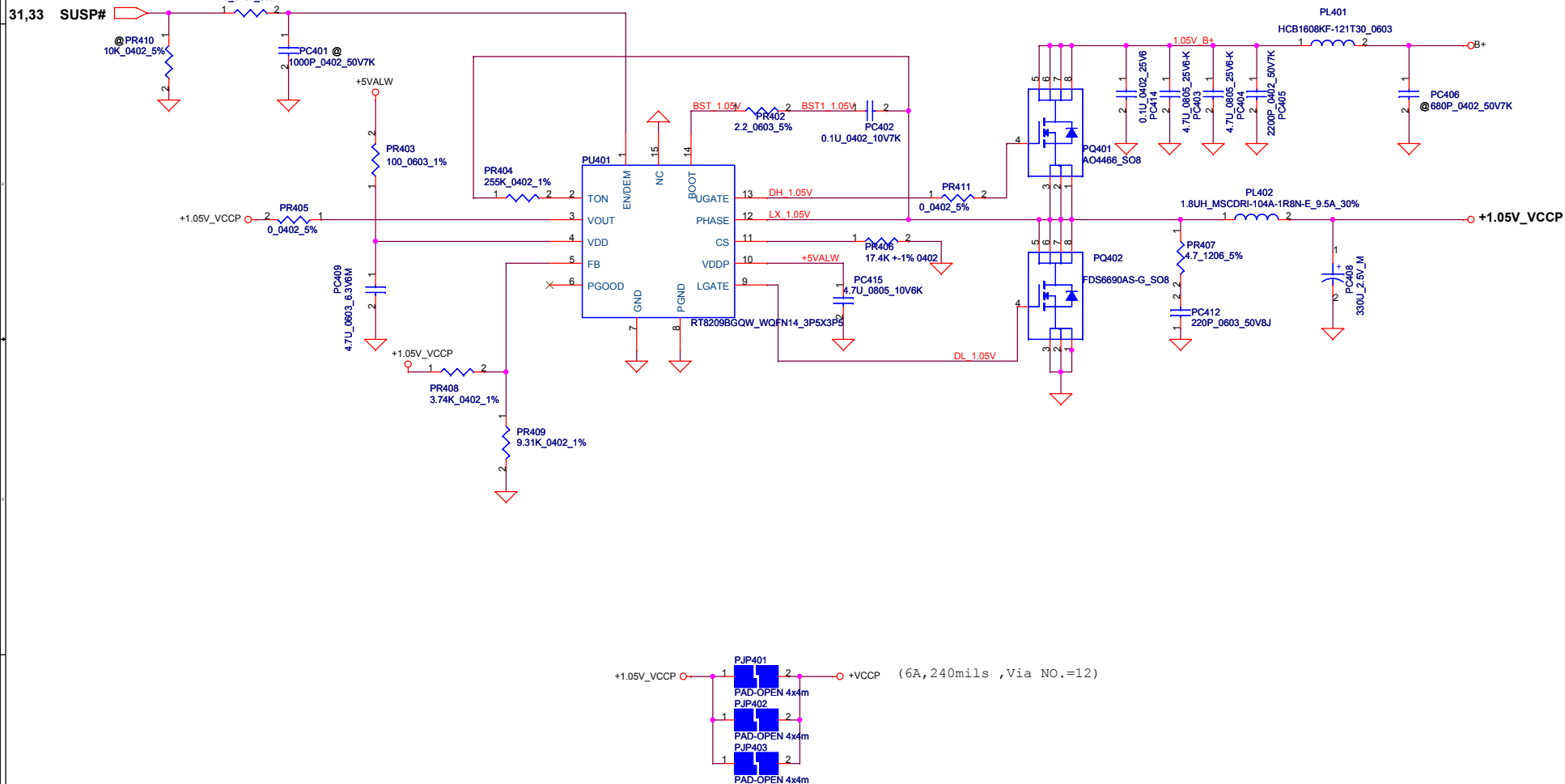
CHGVADJ	CV mode
0V	4V per cell
1.882V	4.2V per cell
3.294V	4.35V per cell

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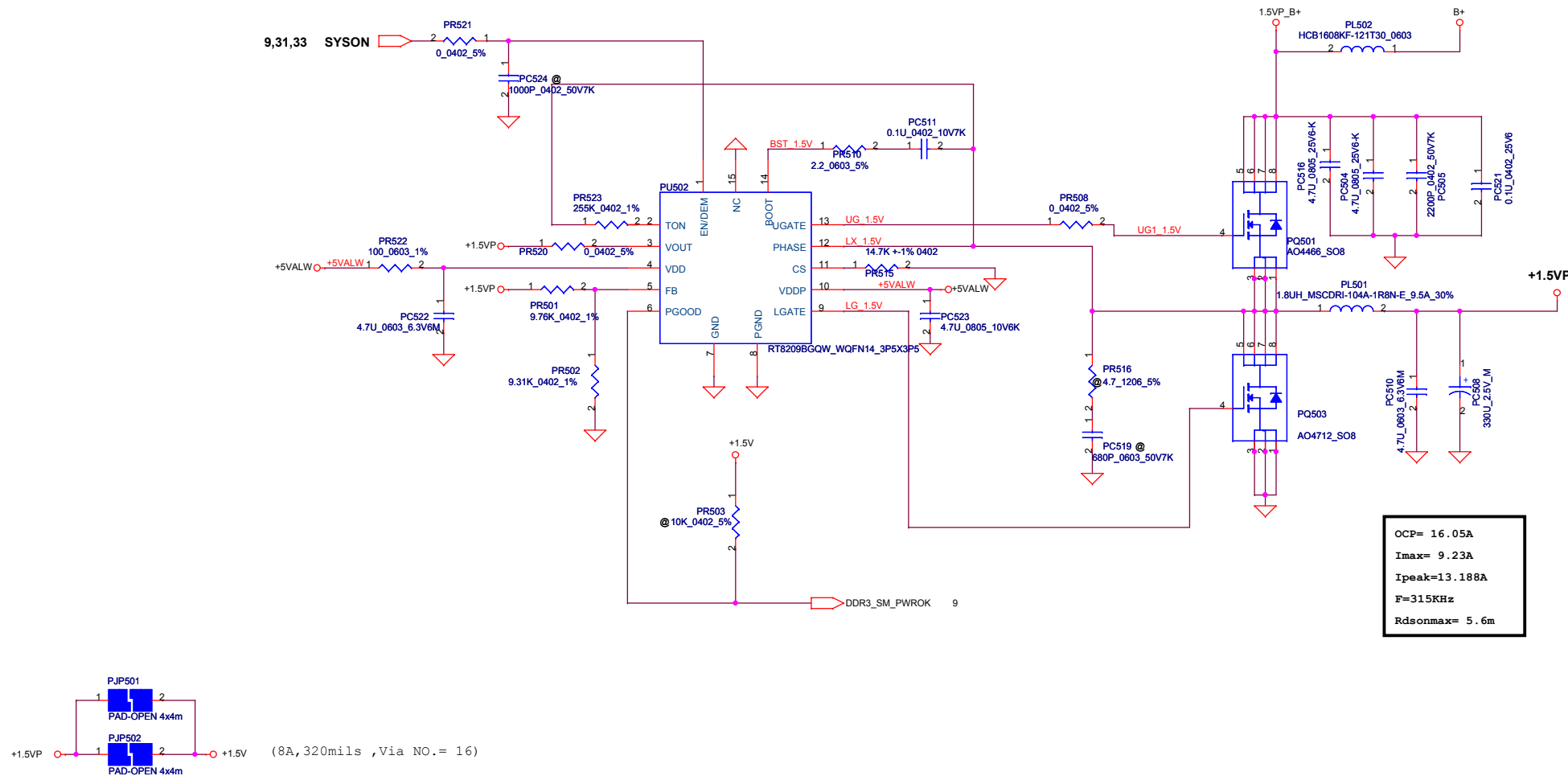


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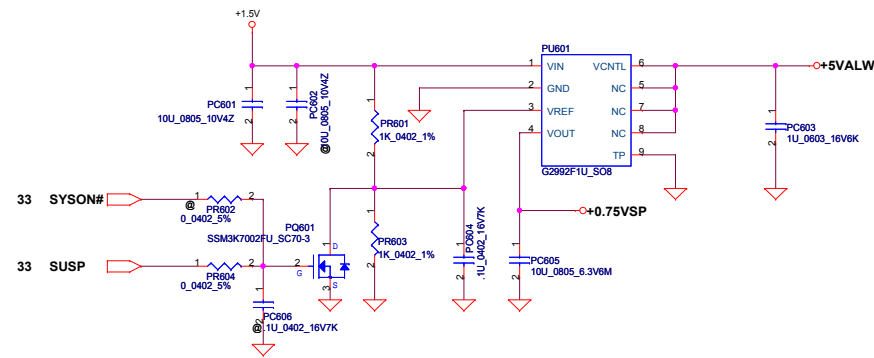
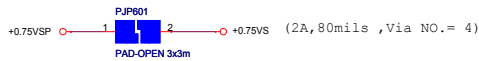
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3.3VALWP/5VALWP Montevina Blade UMA LA4105P			
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Version Change List (P. I. R. List) for Power Circuit

Item	Page#	Reason for change	Description	phase	modify	Rev.
1	36	change charge IC for cost down	change charge IC from TPS24740 to ISL6251	DVT	delete: pu101 and Support Components. add: PU5 and Support Components.	
2	35	Due to ISL6251 can't support pre-charge and Vin detector function	Add pre-charge and Vin detector function	DVT	add PU12	
3	37	for common design	PC302 change to 1U; PC306 change to 4.7U	DVT	PC302 from 0.22U change to 1U PC306 from 10U change to 4.7U	
4	34	Change CPU OTP IC for Cost down	CPU OTP IC from LM358 change to G718	DVT	delete: PU1 and Support Components	
5	41	PH2,PH3 size from 0603 change to 0402 for cost down.	PH2,PH3 size from 0603 change to 0402	DVT	from SL210021F20 change to SL200000V00	
6	39	PC510 size from 0805 change to 0603 for Cost down	PC510 size from 0805 change to 0603	DVT	from SE093475K80 change to SE107475M80	
7	31	for battery can not be charging full issue (notes issue number: ACIC009)	CHGVADJ signal from EC 108pin change to 72pin	DVT	CHGVADJ signal from EC 108pin change to 72pin	
8	41	change load line voltage	change PR130 from 4.02K change to 5.11K	DVT	PR130 from SD034402180 change to SD028511100	
9	41	COST DOWN	Delete CPU_core L-SIDE MOS PQ31 PQ35	DVT	delete: PQ31 PQ35	
10	38	COST DOWN	Change PL402 from 1U to 1.8U	DVT	From SH000008V80 change to SH000008U80	
11	41	COST DOWN	Change CPU_core L-side	DVT	From SB00000GL00 change to SB00000HR00	
12	34/35	COST DOWN	Change PD1/PD2/PD3	DVT	From SC11N414880 change to SC1000001Y80	
13	36	COST DOWN	Change PD13	DVT	From SC1B751V010 change to SCS00000Z00	
14	41	COST DOWN	Change PL13/PL14	DVT	From SH00000F000 change to SH000005680	
15	37	COST DOWN	Change PQ304	DVT	From SB000004J80 change to SB00000AJ00	
16	38	COST DOWN	Change PQ401/PQ402	DVT	PQ401 From SB00000BO00 change to SB00000CG00 PQ402 From SB000009F80 change to SB00000AJ00	
17	39	COST DOWN	Change PQ501/PQ503	DVT	PQ501 From SB00000BO00 change to SB00000CG00 PQ503 From SB000009F80 change to SB00000AJ00	
18	34	COST DOWN	Remove PU2;Connect +3VLP to +CHGRTC	DVT	Remove SA009200010	
19	34	design change	Add PQ1/PQ309 and support circuit	DVT	Add PQ1:SB906100210 PQ309:SB000009610	
20	34	change PU3 support circuit	change from EN0_TRIP to MAINPWON	DVT	change from EN0_TRIP to mainpwon	
21	35	cost down	delete VIN detector circuit	DVT	use ISL6251 VIN detector function	
22	35	change RTCVREF to 62521VREF and support circuit	PR21 change from 499k to 511k PR25 change from 499k to 255k PR39 change from 191k to 150k change RTCVREF to 62521VREF	DVT	PR21 change from SD034499380 to SD034511300 PR25 change from SD034499380 to SD034255300 PR39 change from SD034191380 to SD028150300	
23	35,36	COST DOWN	Change PQ5/PQ23/PQ24/PQ26	DVT	From SB502060000 change to SB000009610	

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Version Change List (P. I. R. List)for Power Circuit

Item	Page #	Reason for change	Description	phase	modify	Rev.
24	36	COST DOWN	change PQ15 to AO4407L	DVT	PQ15 from SB00000DL00 to SB944070010	
25	36	COST DOWN	change PQ27 to AO4468L	DVT	change PQ27 from SB00000CG00 to SB000009510	
26	36	for common design	change ISL6251 ACIN function	DVT	change ISL6251 ACIN function	
27	37	COST DOWN	change PL303 to SH000002L80	DVT	PL303 from SH162100M10 to SH000002L80	
28	37	COST DOWN	change +3/5VALW enable circuit	DVT	change +3/5VALW enable circuit	
29	38	COST DOWN	change PQ402 to FDS6690AS	DVT	PQ402 from SB00000AJ00 to SB000004J10	
30	38	change +1.05V_VCCP OCP setting	change PR406 from 13.7K to 14.7K	DVT	PR406 from SD034137200 to SD034147200	
31	38	COST DOWN	change PC408 from 220U to 330U	DVT	PC408 from SGA20221150 to SF000002Z00	
32	39	COST DOWN	change PL501 from 1UH to 2.2UH	DVT	PL501 from SH000008V80 to SH00000FD10	
33	39	COST DOWN	Change PC508 from Tantalum CAP to Aluminum CAP	DVT	PC508 from SGA00000W00 to SF000002Z00	
34	39	change +1.5VP OCP setting	change PR515 from 8.87K to 14.7K	DVT	PR515 from SD034887180 to SD034147200	
35	41	COST DOWN	Change PQ32,PQ37 from TPCA8023 to TPCA8030	DVT	PQ32,PQ37 from SB00000CK00 to SB00000HL00	
36	42	shortage issue	Change PR406 from 14.7K to 17.4K	PVT	PR406 from SD03414700 to SD03417400	
37	43	Shortage issue	Change PQ15 from AO4407L to S TR P1403	PVT	PQ15 from SB00000DL00 to SB00000DM00	
38	44	COST DOWN cause CPU hang up issue	ADD PQ31,PQ35	PVT	ADD PQ31,PQ35	
39	36	for 030 common design	Change PR91, PR93, PR97	Pre-MP	PR91,PR93,PR97 change to 150K,140K,18.2K	
40	41	For shortage issue	Change CPU_CORE H/L side MOS	Pre-MP	TPCA8030-H change to AON6410 TPCA8036-H change to AON6716L	

Item	Fixed Issue (Reason for change)	PAGE	Modify List	Date	Phase
1	Keyboard can't work.	31	Change R584/R599 pull up PWR from +3valw to +3VL	2009/12/17	DVT
2	LCD can't display.	32	Add (R2406) Lid_sw# pull up to +3VL with 100K.	2009/12/17	DVT
3	Follow Vendor's datasheet.	25	Change Lan chip pin15 to pull down with 10K.	2009/12/17	DVT
4	Follow ID demand.	32	Change Wireless/BT from 2 colore to single colore(Amber)	2010/01/04	DVT
5	To meet KBC PWR plane	26	Change KILL_SW# pull high PWR plane to +3VL	2010/01/04	DVT
6	Follow ID.	31	Delete wow audio/video/dj on EC.	2010/01/04	DVT
7	Follow ME demand.	32	Change JP60 to 8pin.	2010/01/04	DVT
8		17	Delete R123 from BOM	2010/01/04	DVT
9	Kill switch is HW part.	26	Delete CONN@ from schematics.	2010/01/04	DVT
10	SYSON should be 3V.	31	Change R213(8.2K) to CAP(C1415 1U).	2010/01/04	DVT
11	Follow LAN datasheet.	17/25	Delete R191 from Bom,and add R467 to pull up LAN_CLKREQ# with 10k.	2010/01/04	DVT
12		6	Change to 3pin FAN.	2010/01/04	DVT
13	Cost down.	28	Change to 2pin SPK, and change AMP to SA00003X300	2010/01/04	DVT
14	EC common design.	31	add FAN_SPEED at EC pin28, and Kill switch change to pin26.	2010/01/04	DVT
15	Follow panel PWR sequence.	19	Delete C232 from BOM.	2010/01/08	DVT
16		26	Add ESD D8 diode on Kill switch.	2010/01/11	DVT
17	Follow EC common design.	26/31	Change WL_OFF# to EC pin106 control.	2010/01/11	DVT
18	Follow EC common design.	29/31	Change BT_OFF to EC pin99 control.	2010/01/11	DVT
19	Key part demand.	29/26	Change to 8pin BT module.	2010/01/11	DVT
20	For debug.	32	Add PWR button SW on M/B.	2010/01/13	DVT
21	Change WL/BT LED to be always light when WL/BT work .	31/32	Change WL_BT_LED# contral to EC pin86.	2010/01/14	DVT
22	follow PWR's suggestion.	31	Change VCTRL from EC Pin108 to 68	2010/01/14	DVT
23	Follow EC's request.	31	change EC pin108 as EC_SEL.	2010/01/18	DVT
24	Cost down.		change C150/C135 to SF000002000. change C131/3200/94/98/77/115/458 to SF000001500.	2010/01/18	DVT
25	Follow PWR net name	31	change VTRL to CHGVADJ on EC pin68.	2010/01/19	DVT
26	Follow EC common design.	31	Change CHGVADJ from EC pin68 to pin72	2010/01/20	DVT
27	Follow EC common design.	29/31	Add R602/R603/Q14. change BT_OFF to BT_OFF#.	2010/01/20	DVT
28	It is convenient for EC debug.	26/31	EC-TX and EC-RX should connect to WL connector(JP7) 49 pin and 51 pin.	2010/01/20	DVT

Item	Fixed Issue (Reason for change)	PAGE	Modify List	Date	Phase
1	no use ADP_ID.	31	delete location R592(10K).	2010/01/20	DVT
2	no use CIR_IN.	31	delete location R720(10K).	2010/01/20	DVT
3	no use TP_BTN#.	31	delete location R587(10K).	2010/01/20	DVT
4	Modify Gain to 10db.	28	Change C504 to 0.1U.	2010/01/21	DVT
5	Modify Gain to 10db.	28	Change R436/R437 to 30K.	2010/01/21	DVT
6	Modify Gain to 10db.	28	Change R427/R428 to 10K.	2010/01/21	DVT
7	Cost down.	18	Change L2/L3/L4 to SM01000DS00. Change C228/C229/230 to SE07122AC80. Install C225/C226/C227 with SE07122AC80. Modify as KSWAA.	2010/01/22	DVT
8	Modify Gain to 10db.	28	Change C504 back to 0.22U.	2010/01/23	DVT
9	Modify Gain to 10db.	28	Change R429 from 10K to 5K(SD00000HN80).	2010/01/23	DVT
10	Cost down.	19/29	Change Q7/Q105 from SB923010020 to SB934130000, modify as KSWAA.	2010/01/23	DVT
11	Cost down.	28	Change C66/C1450 from SE000004880 to SE053106Z80,	2010/01/23	DVT
12	Cost down.	26/31	Delete R699,R700,R701,R702,R703,R443 (SD028000080)	2010/01/23	DVT
13	Modify the lighteness of LED3.	32	Change R151 from 453ohm to 300ohm (SD028300000)	2010/01/25	DVT
14		28	Uninstall C1492/C1493 (SE071470J80)	2010/01/25	DVT
15		28	Add Location R1281/R1282 at SPK side.(SD013000080)	2010/01/26	DVT
16	Cost down and modify the lighteness of LED.	32	Change R146 from SD034453080 to SD028300000(300ohm)	2010/01/26	DVT
17	Modify the lighteness of LED1/D53.	32	Change R1098/R1101 fromSD028820080 to SD028220080 (220ohm)	2010/01/26	DVT
18	Follow WLAN+BT datasheet.	26	Connect JP7 Pin37/43 to GND.	2010/01/26	DVT
19		17	Delete Location CLRP1.	2010/01/28	DVT
20		32	Add ESD diode D31@ at ON/OFFBTN&ON/OFFBTN_LED#	2010/01/28	DVT
21		29	Uninstall R603.	2010/01/28	DVT
22		18	Change NET C_RED/GRN/BLU to M_RED/GREEN/BLUE.	2010/01/28	DVT
23	Follow EC common desing.	26	Add R1094(SD028100380) to pull down EC_TX with 100kohm.	2010/01/28	DVT
24	Cost down, follow PWR's demand.	8	Change C41/C42@/C43/C44 to SGA19331D10.	2010/01/29	DVT
25	Follow EC common design.	31	uninstall R590.	2010/02/01	DVT
26	Follow EC's suggestion.	22	Add location R347, and uninstall R334.	2010/02/01	DVT
27	EMI demand.	18/19/32	install D31/C223/C224/C302/303.	2010/02/01	DVT
28		19/28	Change Q7/C66 back to SB923010020/SE000004880.	2010/02/02	DVT

Item	Fixed Issue (Reason for change)	PAGE	Modify List	Date	Phase
1	White screen issue.	19	Install R245(10K)-->SD028100280.	2010/03/05	PVT
2		19	Reserve location C71 for BKOFF#	2010/03/05	PVT
3		31	Change R1131 from 22ohm SD028220A80 to 0ohm SD028000080	2010/03/05	PVT
4	Modify the lightness of LED2	32	Modify R120 from SD028220080(220ohm) to SD028100080(100ohm).	2010/03/15	PVT
5	Modify the lightness of LED2	32	Modify R146 from SD028300000(300ohm) to SD028120000(120ohm).	2010/03/15	PVT
6	Modify the lightness of LED1/D53	32	Modify R1098/R1101 from SD028220080(220ohm) to SD00000LK80(90.9ohm).	2010/03/15	PVT
7	Modify the lightness of LED3	32	Modify R151 from SD028300000(300ohm) to SD028150000(150ohm).	2010/03/15	PVT
8	SPK noise issue.	28	Modify R436/r437 from SD014300280(30Kohm) to SD014150280(15Kohm).	2010/03/15	PVT
9	Avoid MIC noise issue.	28	Reserve C304 for +MIC1_VREFO	2010/03/15	PVT
10	Add BT_OFF# pull high to +3VS.	29	Install R603(10K)-->SD028100280.	2010/03/24	Pre_MP
11	Can't disable BT for combo card.	26	Reserve R438 to connect BT_OFF# with JP7 pin5.	2010/03/24	Pre_MP
12	Reserver ICH_susclk for EC's CLK IN.	22/31	Delete T58 and reserver R592.	2010/03/25	Pre_MP
13	Set E0 EC as main source.	31	Install R1093 and uninstall R1091	2010/03/29	Pre_MP
14	Set E0 EC as main source.	31	Change EC P/N to SA00001J5A0(E0)	2010/03/31	Pre_MP
15	Change R249 to 4.99K that have correct description.	31	Change R249 from SD00000HN80 to SD014499180.	2010/03/31	Pre_MP
16	Can't disable BT for combo card.	26/29	Add location Q15(SB570020020), add location R155/R439(SD028000080), add location(SD028100280)	2010/04/01	Pre_MP
17	Reserver ICH_susclk for EC's CLK IN.	31	Reserver location R605	2010/04/08	Pre_MP
18	EMI Request.	25	Add C1409/C1410/C1411(SE070104Z80).	2010/04/08	Pre_MP
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